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# 功率MOS FET

## 功率MOS FET使用时的注意事项

### 1. $V_{GSS}$耐压测量

请不要进行$V_{GSS}$（栅极/源极电压）的测量。击穿时会产生负电阻特性，有可能引起振荡并损坏器件。

### 2. 观察源极接地输出静态特性时的注意事项

(1) 观察源极接地输出静态特性时，根据曲线绘图仪的种类（输入电容/电阻不同）不同，有可能产生振荡，并导致器件损坏。有效的措施是在栅极连接约10kΩ的外部串联电阻。

(1) 用X–Y记录器描绘源极接地输出静态特性时，为防止振荡请给栅极连接约10kΩ的串联电阻或在栅极/源极之间放入约0.5μF的电容。

### 3. 对于异常振荡的注意事项

(1) 进行电路试验时，为防止异常振荡，在熟练使用以前，推荐给栅极连接100Ω～2kΩ的串联电阻。

(2) 使用源极输出电路时，为防止异常振荡，推荐在漏极附近电源与地线之间连接约100μF的电容。

### 4. 为防止静电破坏使用功率MOS FET时的注意事项

为防止静电破坏请注意以下几点：

(1) 对器件进行操作时，请采用人体接地方式。
人体接地的例子如图1所示。

(2) 对器件进行操作时的工作台上铺有金属板，请将金属板接地。

(3) 用曲线绘图仪等测量仪器进行单个器件的检查时，请将测量仪器接地。

(4) 为防止对器件外加烙铁焊接的泄漏电压，请将烙铁焊接的烙铁头接地（尽量使用低电压烙铁焊接）。

(5) 在电路板的运输中，请使用导电性片材制作的包装材料。在栅极/源极之间已通过电阻等连接的情况下，不作此限。因此，推荐首先安装栅极/源极之间的元件。

(6) 请避免直接将器件装入塑料盒或塑料袋中，而使用导电性容器或铝箔等。

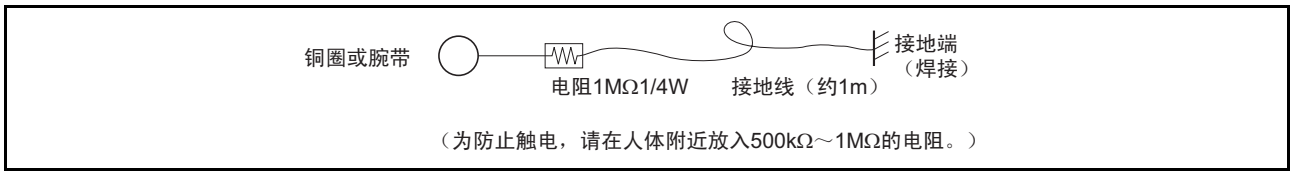



图1　人体接地的例子

### 5. 关于在功率MOS FET中产生问题时的耐压波形

当使用功率MOS FET时，对于客户在设计中所用器件的最大额定值、工作电源电压范围、散热特性/安装条件等诸多条件，请在茂钿规定的保证范围内使用，如果使用时超出了规定的保证范围，并因此造成故障及事故时，本公司概不负责。

但是，即使在保证范围内使用时，也要考虑半导体产品可能会出现的故障率，并事先掌握和研究此时的故障模式。另外，在功率MOS FET的生产方面，茂钿尽力保证其安全，但不排除在生产过程中，可能会因为某种问题，比如由于电路板安装时的热应力及功能确认测试等，使产品受到某种应力而导致故障。因此，请在设计阶段充分考虑上述情况，积极采取自动保险装置等系统方面的对策，以避免因茂钿产品的故障及误动作而导致人身事故/火灾事故等重大损失。

另外，产品产生问题时的耐压波形如下所示，该图为代表状态下的波形模式略图。详细情况因产品的不同而异，望用户周知。

正常产品的特性 （2SK2869时）

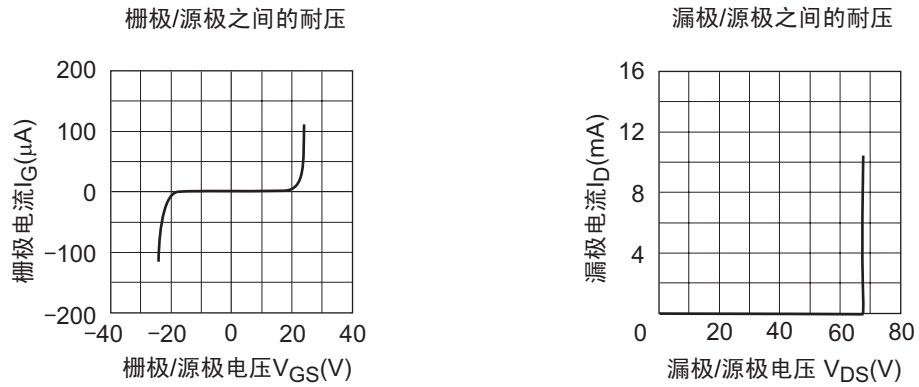
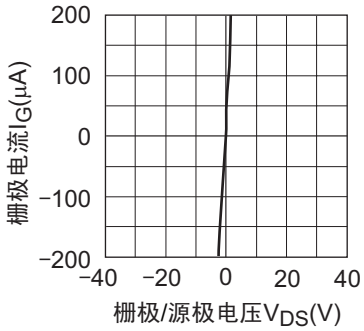


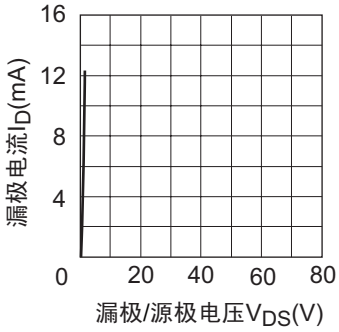

图2　功率MOS FET正常产品的耐压波形

问题模式1（芯片损坏）（但是，要确保各引脚的芯片连接线以及与安装电路板的连接）

栅极/源极之间的耐压

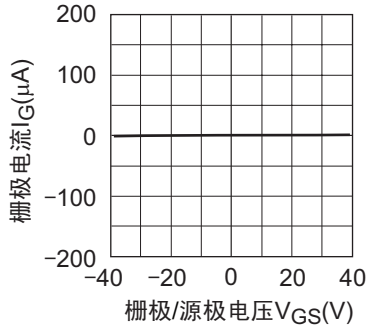



漏极/源极之间的耐压

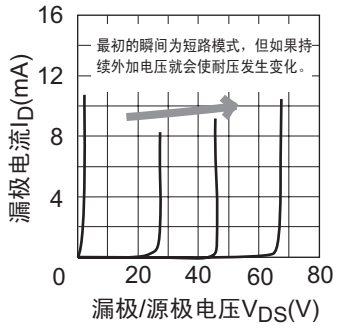



问题模式2（芯片正常－栅极引脚的芯片连接线断裂或未与安装电路板接触）

栅极/源极之间的耐压

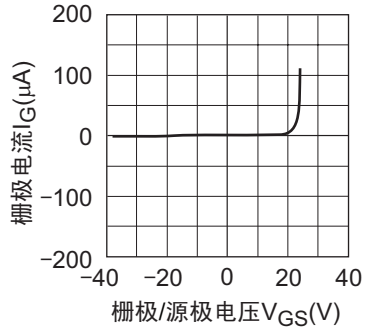



漏极/源极之间的耐压




问题模式3（芯片正常－源极引脚的芯片连接线断裂或未与安装电路板接触）

栅极/源极之间的耐压




漏极/源极之间的耐压

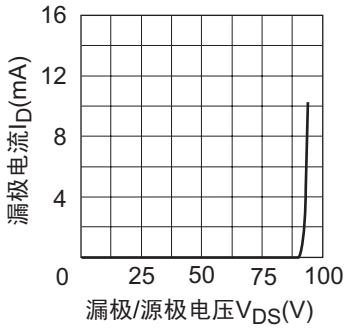
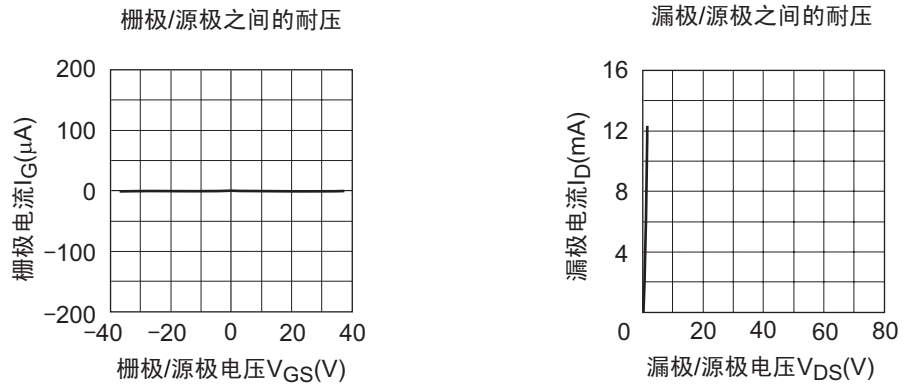



图3　功率MOS FET产生问题时的耐压波形(1)

问题模式4 （芯片损坏－栅极引脚的芯片连接线断裂或未与安装电路板接触）




问题模式5 （芯片损坏－源极引脚的芯片连接线断裂或未与安装电路板接触）

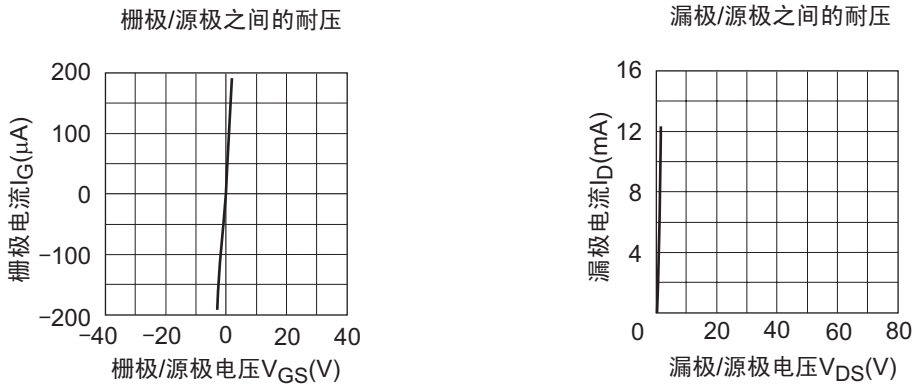



图3　功率MOS FET产生问题时的耐压波形(2)

## 6. 对于高速开关时产生峰值电压的注意事项

将功率 MOS FET 用作开关时，要考虑开关器件的负载成为感性负载的情况。此时，由于功率 MOS FET 处于极高速状态，所以当切断器件电源时，电路中的电感有可能引起瞬间的过大峰值电压。下面对漏极/源极之间产生峰值电压的注意事项进行说明。

图4(a)表示无钳位二极管的感性负载开关工作情况。此时，产生由Ldi/dt决定的过渡电压，并且如果该过渡电压超出器件的耐压就可能损坏器件。

图 4(b) 是带有钳位二极管的电路，即使负载被钳制，在实际电路中也存在由布线引起的电感。该电感主要是由钳位二极管的阳极与功率MOS FET漏极之间的布线以及到电源的布线而引起的。因此在高速、大电流状态下进行开关工作时，即使想进行钳制也会因外加超出器件耐压的实际峰值电压而损坏器件。特别是因为该峰值电压会随着电流的增大而增大，所以实际上必须事先在电源电压、负载电流的最坏条件下通过高速示波器确认电压波形。

关于峰值电压的对策如下所示：

(1) 通过尽量缩短电路布线，将残余电感控制在最小限度 （使用双扭线作为电源线的引线，并将电流环路的面积控制在最小范围）。
(2) 在漏极/源极引脚根部连接用于吸收电涌的雪崩二极管，以吸收峰值电压 （图4(c)）。
(3) 在漏极/源极之间连接CR缓冲器，以控制峰值电压 （图4(d)）。

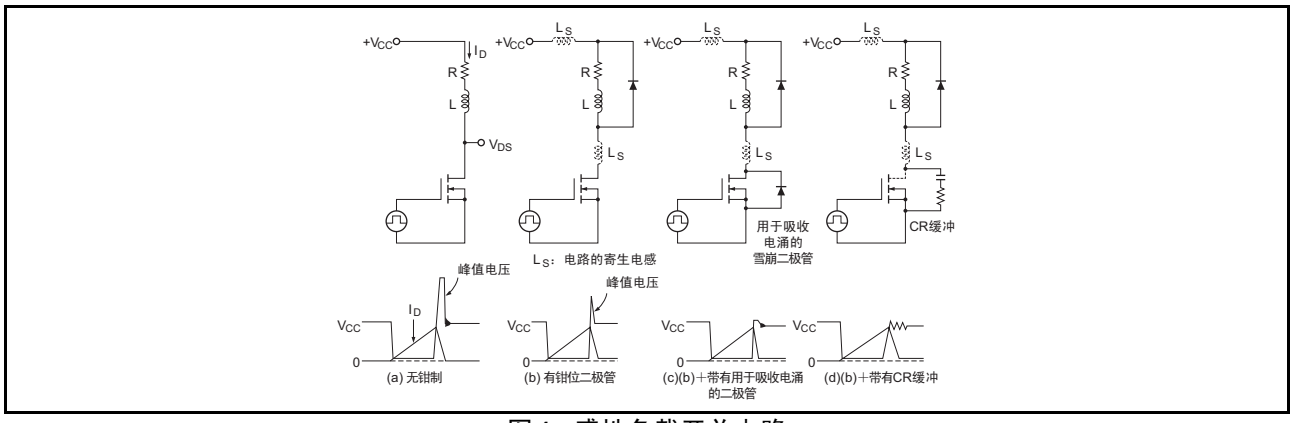



图4　感性负载开关电路

必须注意峰值电压的另一用途为马达控制电路。图5表示基本的马达控制电路，其工作时的波形如图6所示。

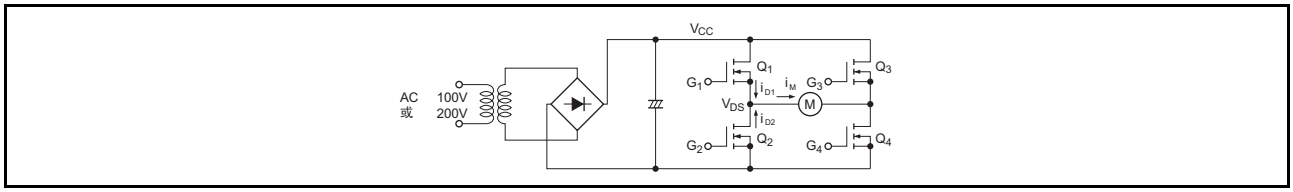



图5　马达控制基本电路

图6的波形，是在图5的电路中$Q_2$和$Q_3$为OFF、$Q_1$和$Q_4$为ON、且$Q_4$在$Q_1$斩波期间总为ON时的波形。该波形说明了峰值电压的产生过程。

向$G_1$输入栅极驱动信号，并接通$Q_1$、通入$i_{D1}$。如果切断$Q_1$的电流$i_{D1}$，由马达电感积累的能量就会通过$Q_2$的内部二极管产生再生电流iF。在该状态下如果接通$Q_1$，因受$Q_2$内部二极管反向恢复时间$t_{rr}$的影响，$Q_2$就会变成导通状态，并产生过大的冲击电流（恢复电流）$i_{Dr}$，该电流也流向$Q_1$。然后在该$i_{Dr}$恢复期间（图中斜线部分），如果存在电路的寄生电感LS，就会产生由LS $di_{Dr}/dt$决定的峰值电压。所以必须尽量减小该峰值电压。采取的措施如前面所述：

(1) 要充分注意电路的布线，将残余电感控制在最小限度（使用双扭线作为电源线的引线，并减小电流环路的面积。另外，为避免产生电感，最好直接连接$Q_1$源极和$Q_2$漏极的布线、以及$Q_3$源极和$Q_4$漏极的布线。并联时也必须同样注意）。电源线的引线电感无论如何都有残余时，也可采取在$Q_1$漏极和$Q_2$源极引脚根部、以及在$Q_3$漏极和$Q_4$源极引脚根部连接C=0.1～1.0μF电容的有效措施。更改各个布线条件时的波形请参照图7所示的照片(A)～(E)。

(2) 在漏极/源极之间连接CR缓冲器以控制峰值电压。

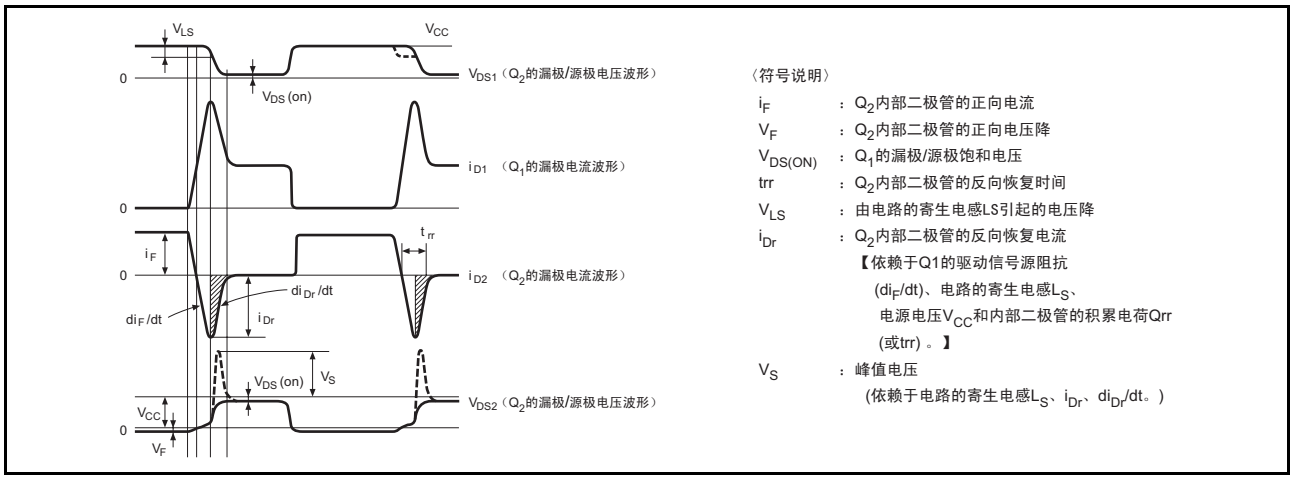



图6 马达控制工作时的波形

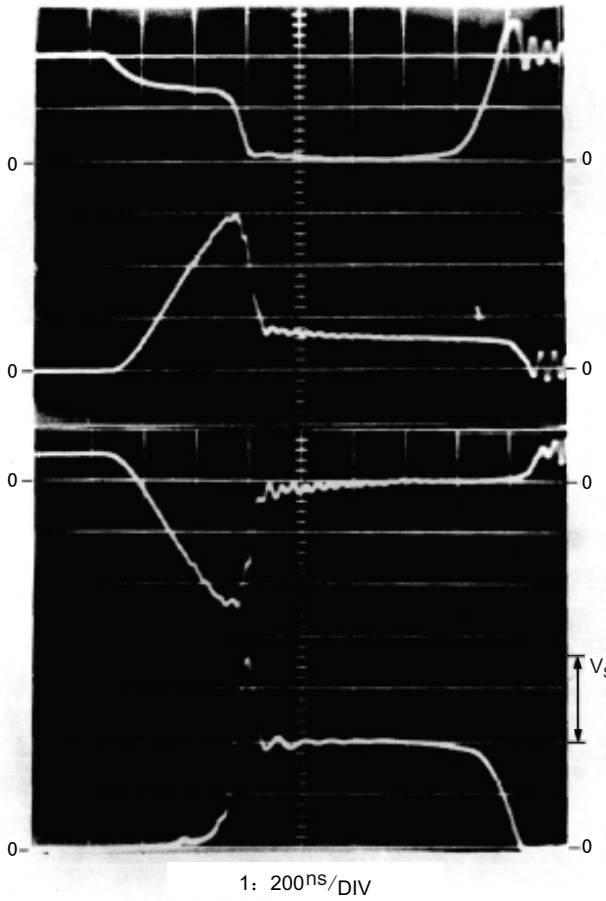
## 7. 对于电路布局、布线的注意事项

在高速开关时，电路中的寄生电感可能导致瞬间的过大电压、开关速度低（特别是栅极的引线电感）以及多个并联的器件之间电流不平衡，甚至产生异常振荡。为防止上述问题的发生，要尽量缩短电源线、栅极/源极之间引线的布线，将电流环路的面积设为最小，并使用双扭线等。另外，通过局部安装去藕电容也可减小残余电感的影响。

为减小并联时功率MOS FET的电流差异，要尽量使电路的布局对称。

另外，多个器件并联时，通过在栅极的连接处放置小型铁氧体磁珠或在各功率MOS FET栅极处插入约50～150Ω的串联电阻可防止异常振荡。

测量条件 $\left\{\begin{array}{l} V_{CC}=100V、f=20kHz \\ V_{GS}=\begin{array}{l}+15V\\-10V\end{array}、I_D=5A、{di}/{dt}=80{A}/{\mu s}\end{array}\right.$




$V_{DS1}$：$50^{V}/_{DIV}$
（$Q_1$的漏极/源极电压波形）

$i_{D1}$：$10^{A}/_{DIV}$
（$Q_1$的漏极电流波形）

$i_{D2}$：$10^{A}/_{DIV}$
（$Q_2$的漏极电流波形）

$V_{DS2}$：$50^{V}/_{DIV}$
（$Q_2$的漏极/源极电压波形）

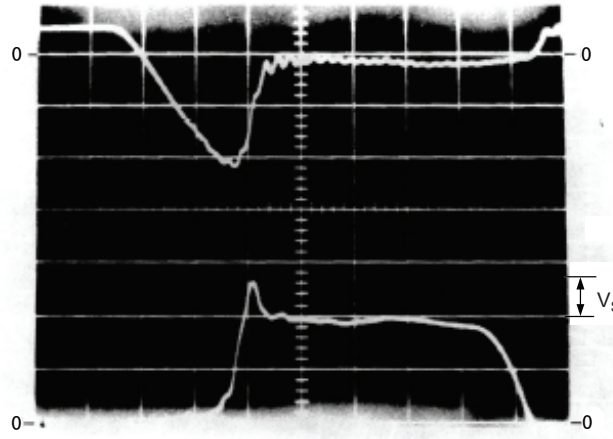
1：$200^{ns}/_{DIV}$

照 片 Ⓐ

〔布 线 条 件〕

①$V_{CC}$～$D_1/S_2$
是双扭线
（$L_S$≈170nH）

②$S_1$引脚-$D_2$引脚
间10cm引线
（$L_S$≈100nH）




$i_{D2}$

$V_{DS2}$

照 片 Ⓑ

〔布 线 条 件〕

①$V_{CC}$～$D_1/S_2$
是双扭线
（$L_S$≈170nH）

②$S_1$引脚-$D_2$引脚间
用铜板连接
（$L_S$≈25nH）

图7 使用2SK401时FET$Q_1$、$Q_2$的电压、电流波形照片 （接下页）

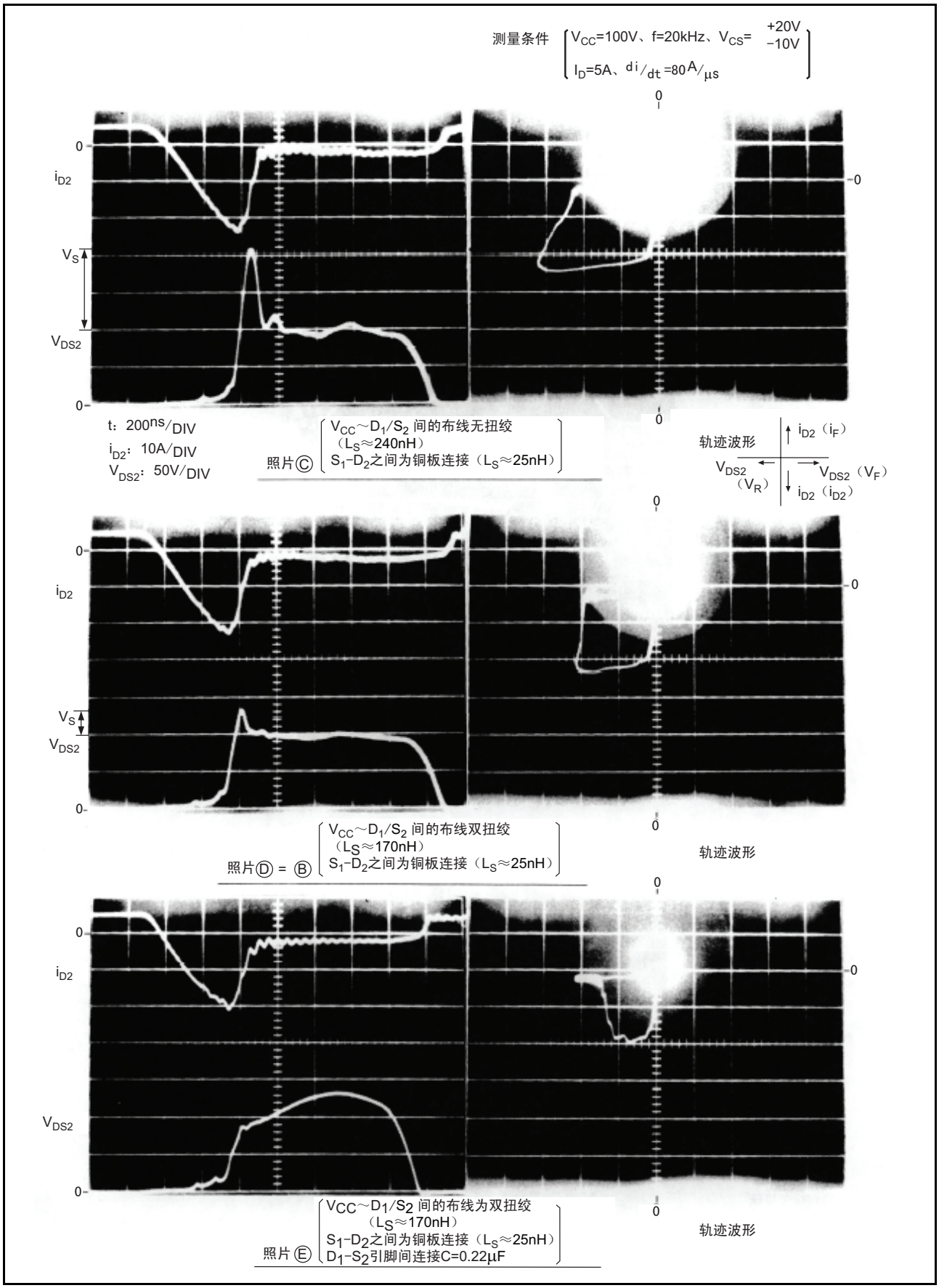


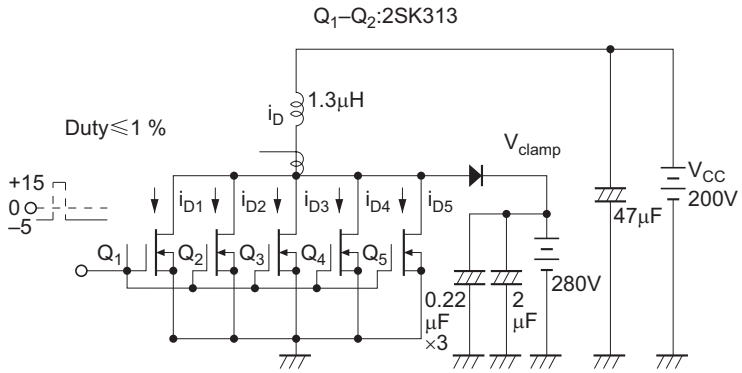

图7　使用2SK401时FET$Q_2$的电压、电流波形

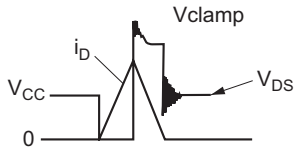
## 8. 并联时的注意事项

### 8.1 高速开关工作中并联时的电流差异
### （对于并联时的电路布局/布线的注意事项）

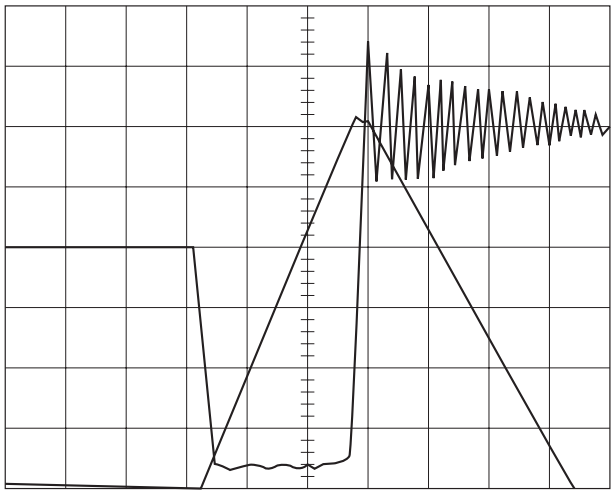
功率 MOS FET 用于放电加工机等时，将多个器件并联以得到大电流。此时，由于高速开关工作 (f=200 ～ 500kHz)，电路中的寄生电感有可能导致各器件之间的瞬间峰值电压和电流差异。

前者可采取尽量缩短或加粗布线的对策，对于后者还必需研究电路的布线、布局。通过图8的试验电路，试对图9和图10的2种布线方法及并联时的电流差异进行测量。




波形



试验电路的波形（$I_D$=30A时）
$V_{DS}$=50V/DIV、$I_D$=5 A/DIV、t=100ns/DIV

图8 试验电路、波形

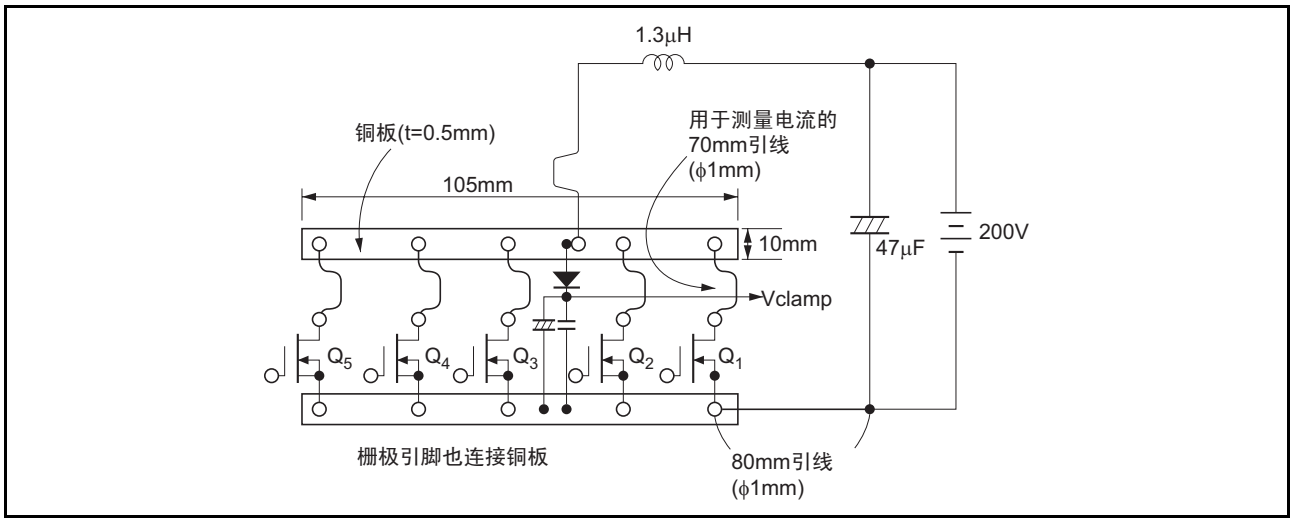



图9　布线方法(I)

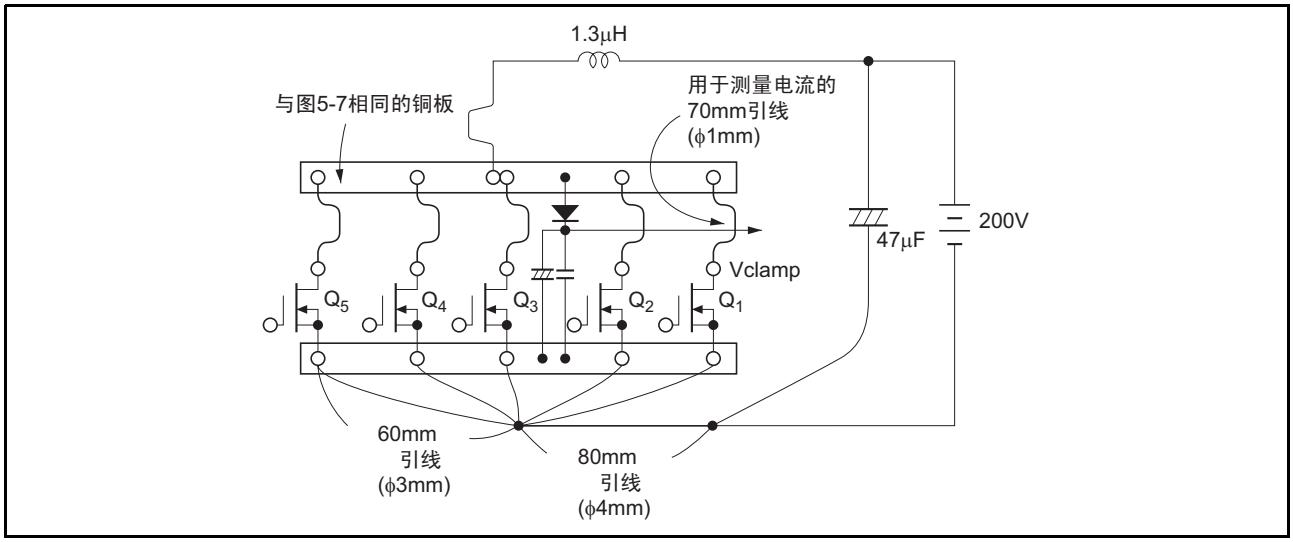



图10　布线方法(II)

表1　样品2SK313的各个特性和不同电路布局、布线方法时的电流差异数据

| No. | 项目 | | | | | | |
|---|---|---|---|---|---|---|---|
| | 电特性 | | | | | 电流分配 （$i_D$=30A时） | |
| | (V)<br>$V_{(BR)DSS}$<br>$I_D$=10mA<br>$V_{GS}$=0 | (nA)<br>$I_{DSS}$<br>$V_{DS}$=360V<br>$V_{GS}$=0 | (V)<br>Vth<br>$V_{DS}$=10V<br>$I_D$=1mA | (S)<br>$g_m$<br>$V_{DS}$=10V<br>$I_D$=6A | (Ω)<br>Ron<br>$V_{GS}$=15V<br>$I_D$=6A | 布线方法<br>(I) | 布线方法<br>(II) |
| $Q_1$ | 502 | 9.0 | 2.98 | 3.31 | 0.66 | $i_{D1}$≈8.0A | 6.0A |
| $Q_2$ | 499 | 133 | 3.10 | 3.18 | 0.65 | $i_{D2}$≈6.5 | 6.0 |
| $Q_3$ | 502 | 27 | 3.11 | 3.19 | 0.65 | $i_{D3}$≈5.7 | 5.8 |
| $Q_4$ | 487 | 5.0 | 3.01 | 3.28 | 0.61 | $i_{D4}$≈5.0 | 6.0 |
| $Q_5$ | 476 | 17 | 3.02 | 3.29 | 0.58 | $i_{D5}$≈4.8 | 6.2 |

表1表示所使用的5个FET的主要特性和对应于各个布线方法的电流差异数据。

如表1所示，在图9的布线方法(I)中，$Q_1$和$Q_2$的漏极及源极布线电感变小，$Q_1$的电流最大，约为8.0A，而布线电感较大的$Q_5$的电流最小，约为4.8A。这样，器件之间的电流差异增大。（参照图11的波形照片）因此，在图10的布线方法(II)中，通过对源极进行相同布线并平衡布线电感的方法，可大致平衡器件之间的电流如表1及图17所示的波形照片。即，即使具备Vth、gm、Ron等特性，根据电路布线、布局条件的不同，各器件之间的电流值也大不相同。因此，必须对各个器件的电路进行相同布线并对称布局，以减小并联时功率MOS FET的电流差异。

$V_{DS}$=50V/DIV、$I_D$=2A/DIV、t=100ns/DIV

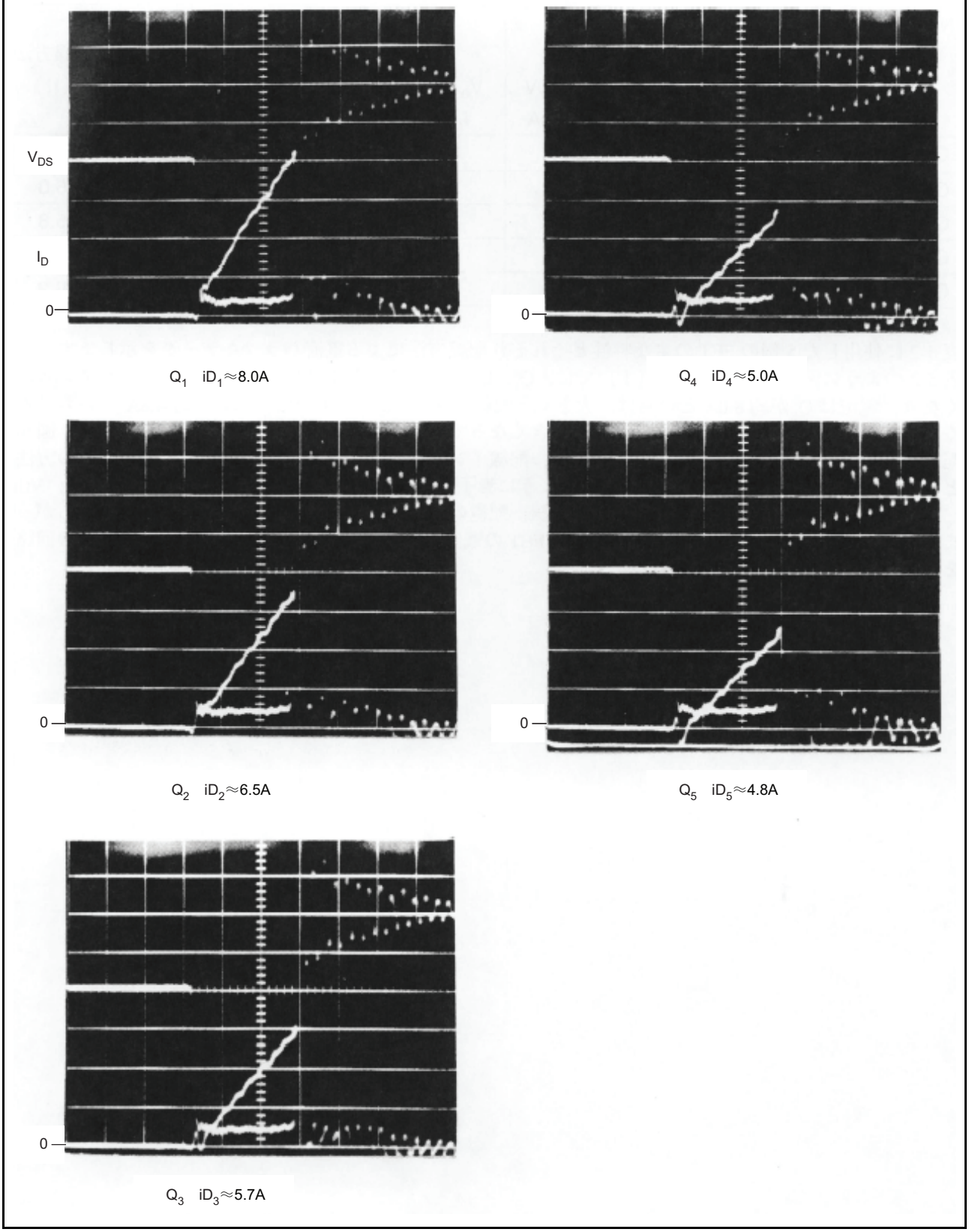
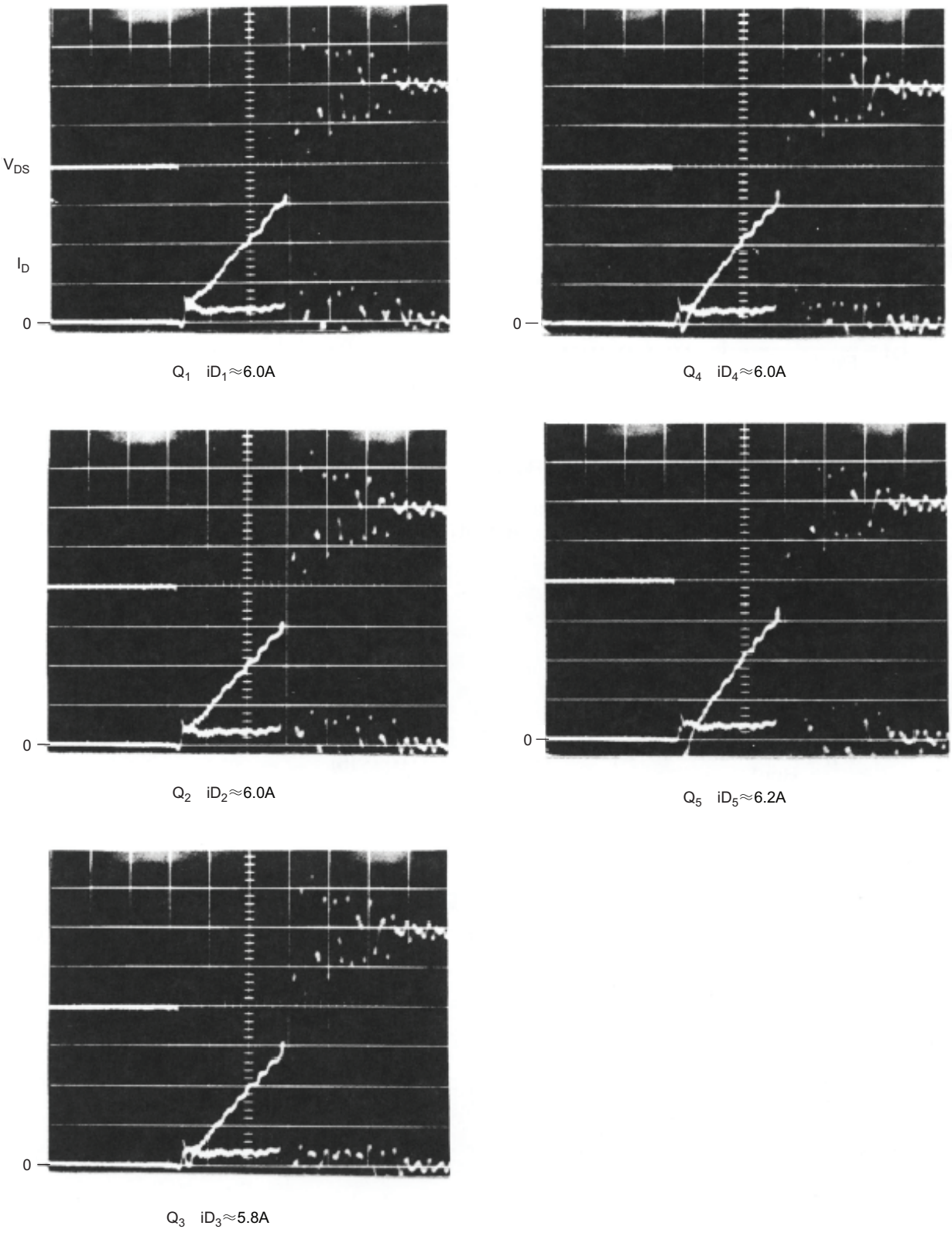



图11　2SK313 L负载开关并联工作时的电流分配 （布线方法(I)）

$V_{DS}$=50V/DIV、$I_D$=2A/DIV、t=100ns/DIV




$Q_1$ $iD_1$≈6.0A

$Q_4$ $iD_4$≈6.0A

$Q_2$ $iD_2$≈6.0A

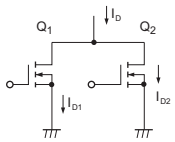
$Q_5$ $iD_5$≈6.2A

$Q_3$ $iD_3$≈5.8A

图12 2SK313 L负载开关并联工作时的电流分配 （布线方法(II)）

## 8.2 并联时由通态电阻差异所产生的损耗差异 （仅供参照）

(1) 损耗的计算




〔条件、假定〕

Tc≈Tj=25°C

$Q_1$的Ron：$Ron_1$

$Q_2$的Ron：$Ron_2=n\ Ron_1(n>1)$

$Q_1$的损耗：$P_{D1}$

$Q_2$的损耗：$P_{D2}$

$$I_{D1}=\frac{n\,Ron1}{Ron1+n\,Ron1}I_D \cdots\cdots(1)$$

$$I_{D2}=\frac{Ron1}{Ron1+n\,Ron1}I_D \cdots\cdots(2)$$

$$P_{D1}=I_{D1}^2\cdot Ron1=\left(\frac{n\,Ron1}{Ron1+n\,Ron1}I_D\right)^2\cdot Ron1 \cdots\cdots(3)$$

$$P_{D2}=I_{D2}^2\cdot n\,Ron1=\left(\frac{Ron1}{Ron1+n\,Ron1}I_D\right)^2\cdot n\,Ron1 \cdots\cdots(4)$$

求$P_{D1}$与$P_{D2}$的比为，

$$\frac{P_{D1}}{P_{D2}}=\frac{\dfrac{n^2\cdot Ron1^2}{(Ron1+n\,Ron1)^2}\cdot I_D^2\cdot Ron1}{\dfrac{Ron1^2}{(Ron1+n\,Ron1)^2}\cdot I_D^2\cdot n\cdot Ron1}$$

$$=n=\frac{Ron2}{Ron1} \cdots\cdots(5)$$

此公式说明， Ron小的$Q_1$损耗$P_{D1}$比$Q_2$的损耗$P_{D2}$大n （$Ron_2/Ron_1$）倍 （其中$Ron_2>Ron_1$）。

因此，根据Ron的比不同，并联时的损耗会有所变化。图13、图14表示在Tc=25°C时以$Ron_2/Ron_1$为参数计算的损耗差异。单体的最大容许损耗为$P_D$=100W （Tc=25°C， 2SK557、 2SK560的例子），但在并联的情况下，由于Ron小的器件损耗增大，所以必须将单体的最大容许损耗控制在最大额定值以内。

例如，在2SK560中$Ron_1$=0.3Ω （小）、 $Ron_2$=0.375Ω （大）时，$\frac{Ron\,2}{Ron\,1}$ =1.25，由此可以算出如果要在额定值内使用Ron小的器件，必须进行80%或80%以上的减额。

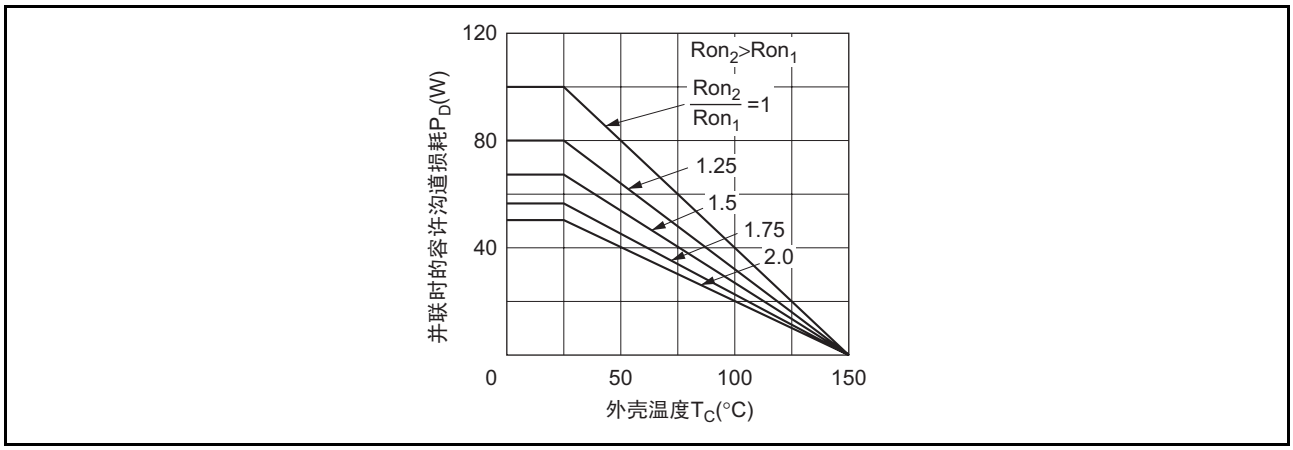



图13　2SK560并联时的PD-TC （2SK560的例子）

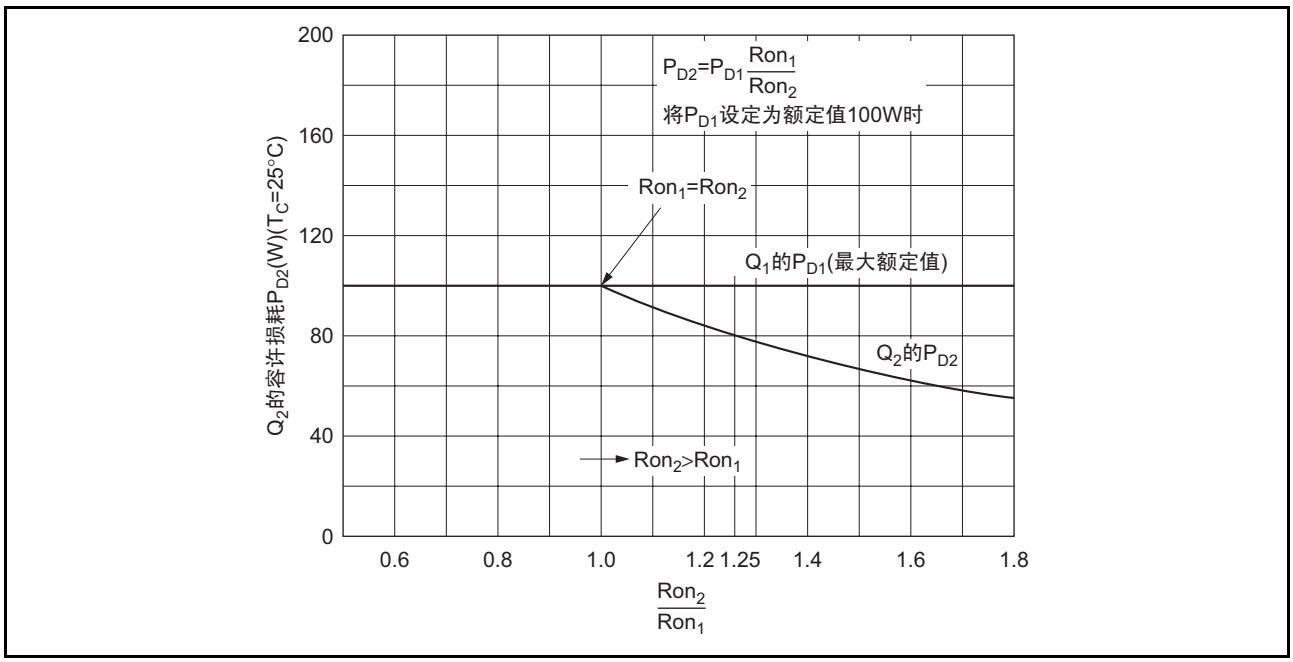



图14　并联时由通态电阻差异产生的容许损耗减额 （2SK560的例子）

但是，实际上如果外加功率， $Q_1$、 $Q_2$ 和结温就上升 （如下列公式所示） ，由于 Ron 小的 $Q_1$ 上升到高于 $Q_2$($Tj_1$>$Tj_2$)，因此，与$Ron_2$相比， $Ron_1$的温度上升幅度要大。在Tc≈Tj<25°C的条件下， $Ron_2/Ron_1$得到补正，而损耗和$I_D$也开始趋于平衡。

$$\Delta Tj_1 = \theta ch-c \cdot P_{D1}$$

$$= \theta ch-c \cdot \frac{Ron_2}{Ron_1} P_{D2} \cdots\cdots(6)$$

$$\Delta Tj_2 = \theta ch-c \cdot P_{D2} \cdots\cdots(7)$$

$$\therefore \Delta Tj_1 = \frac{Ron_2}{Ron_1} \cdot \Delta Tj_2 \text{（其中 } Ron_2>Ron_1\text{）} \cdots\cdots(8)$$

例如，在2SK560中当$Ron_1$=0.3Ω（小）、 $Ron_2$=0.375Ω（大）时，图15中的Ron-Tc特性补正为原来的结果（如表2所示）。

表2　Tj上升时的$Ron_2/Ron_1$补正例子 （2SK560的例子）

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| FET $Q_2$ | $\Delta Tj_2$ | (°C) | 0 | 25 | 50 | 75 | 100 | 125 |
| | $Tj_2=Tc+\Delta Tj_2$ | (°C) | 25 | 50 | 75 | 100 | 125 | 150 |
| | $Ron_2(T)$ | (Ω) | 0.375 | 0.47 | 0.57 | 0.67 | 0.77 | 0.87 |
| FET $Q_1$ | $\Delta Tj_1=n\Delta Tj_2$ | (°C) | 0 | (29.5)<br>31.2 | (57.0)<br>62.5 | (84.0)<br>93.8 | (110)<br>125 | 156.3 |
| | $Tj_1=T_C+Tj_1$ | (°C) | 25 | (54.5)<br>56.3 | (82.0)<br>87.5 | (109)<br>118.8 | (135)<br>150 | 181.2 |
| | $Ron_1(T)$ | (Ω) | 0.30 | (0.39)<br>0.40 | (0.48)<br>0.50 | (0.57)<br>0.60 | (0.65)<br>0.70 | — |
| 补正$Ron_2/Ron_1=n$ | | | 1.25 | (1.21)<br>1.81 | (1.19)<br>1.14 | (1.18)<br>1.12 | (1.18)<br>1.10 | — |

【注】1. (　)内的数字为补正$\Delta Tj_1=n\Delta Tj_2$的n时数值。
2. $T_C$=25°C

图15、图16表示由Ron差异引起结温上升ΔTj的差异。单体的容许结温上升ΔTj在Tc=25°C时最大为125°C.，因为上述的损耗根据 Ron 的比进行变化，所以 ΔTj 也随之变化。但是，实际上如果外加与损耗时相同的功率，$Ron_2/Ron_1$的比就会得到补正，并趋于平衡 （参照表2）。

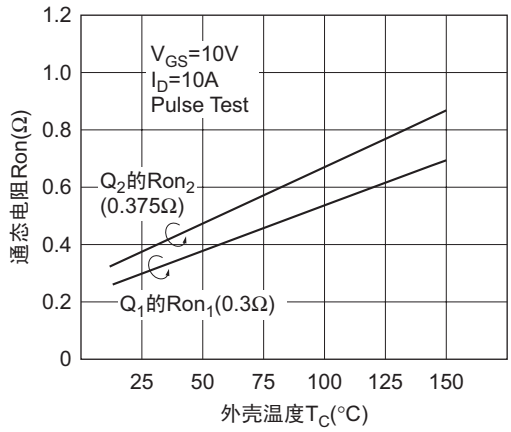



图15　Ron-TC特性

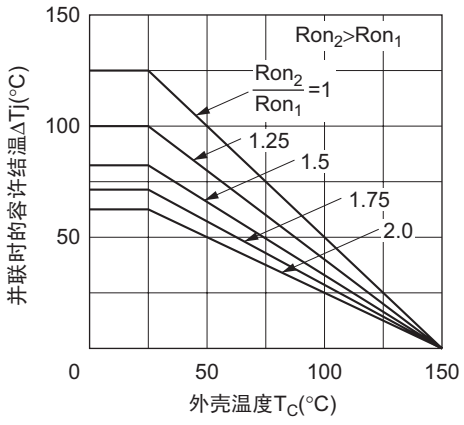



图16　并联时的结温减额例子

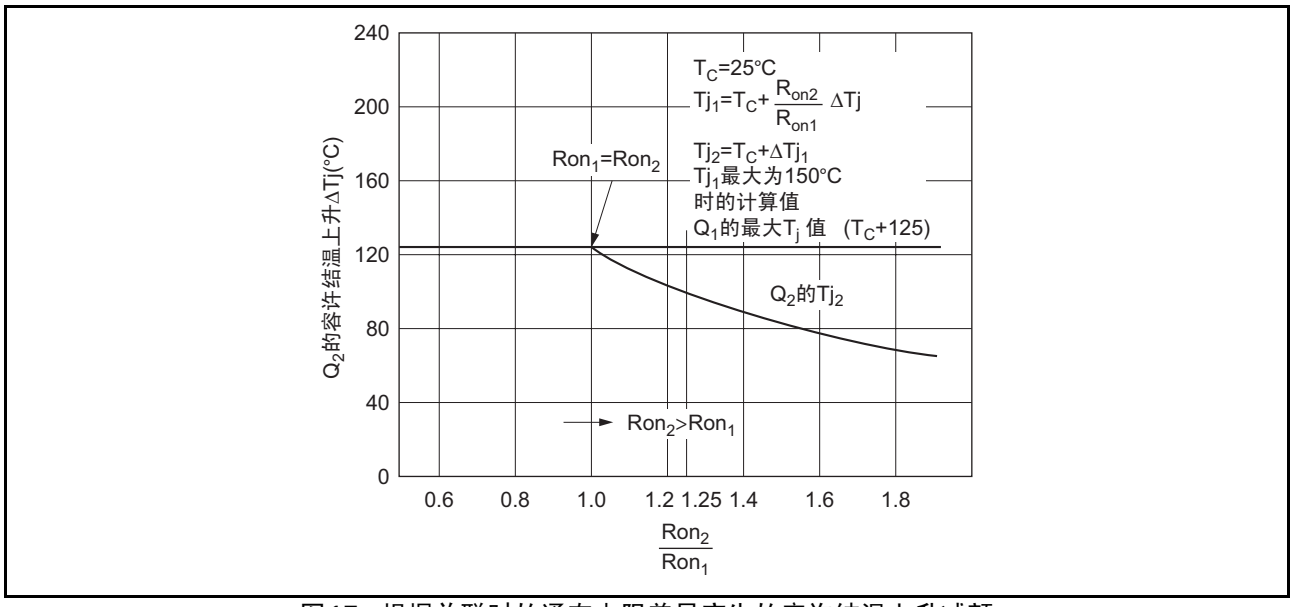



图17　根据并联时的通态电阻差异产生的容许结温上升减额
（2SK560的例子）

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## Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.