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功率MOS FET

结构与特点

茂钿科技功率MOS FET具有D系列（垂直结构）和S系列（水平结构）。其结构分别如图1和图2所示。两者在特性上稍有差别，但都拥有功率MOS FET在本质上的优良特性，具体内容如下：

- 无载流子的积累现象，具有优良的频率特性和开关特性。
- 无电流集中，破坏耐量大。
- 为电压控制器件，驱动功率小。

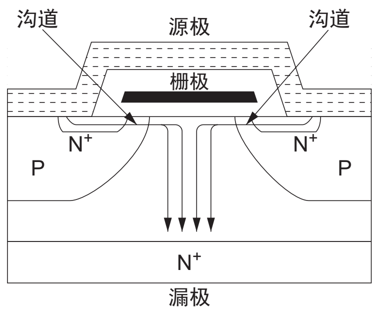

图1　D系列（垂直）的结构（N沟道）

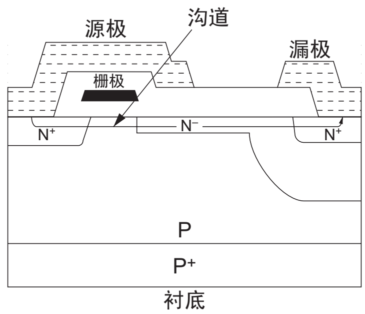

图2　S系列（水平）的结构（N沟道）

为了解功率MOS FET的结构及特性，下面介绍一下基本的N沟道MOS FET结构和工作。

N沟道MOS FET的基本结构如图3所示。因为控制电流的栅电极被氧化膜包围，所以该结构称为MOS结构。源极指的是带电粒子（这里为电子）源，漏极指的是电子的排出口。

如果对栅电极施加正电压，栅极正下方的P层就会反转形成沟道，并且漏极电流由漏极流向源极，这就是MOS FET的工作方式（P沟道与之相反）。

如果在漏极/源极之间施加电压，沟道内的电子就向漏极移动，并产生漏极电流。

在栅极电压为0V时，产生漏极电流的FET称为耗尽型（常开型），不产生漏极电流的FET称为增强型（常关型）。茂钿科技功率MOS FET全部为增强型（常开型）。

将漏极电流产生时的栅极电压称为栅极截止电压$V_{GS(off)}$（图4）。

通常I_{DS}–V_{GS}为2次相关关系。该曲线的斜度为相互电导gm(=$\Delta I_{DS}/\Delta V_{GS}$)，表示放大的尺寸。

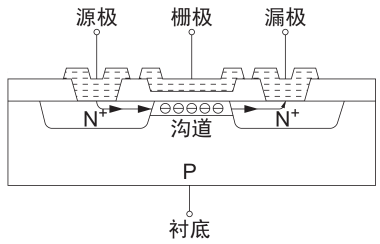

图3 MOS FET的基本结构 （N沟道）

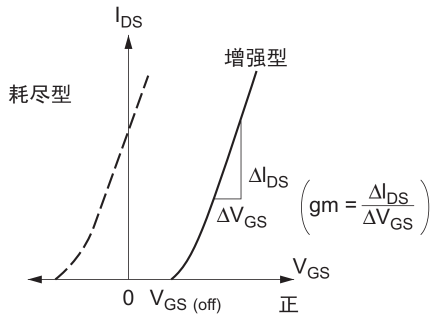

图4 传输特性

漏极耐压由图3所示的漏极N^+区域和栅电极之间的结构决定。由于漏极N^+区域与栅电极的距离很近，中间只隔着很薄的栅极氧化膜，这样会在两者之间产生强电场的集中，因此不能形成较强的漏极电压。普通MOS FET的耐压值为20～30V。

通过扩大该漏极N^+区域和栅电极的距离以缓和电场集中，可提高漏极耐压。此时，在漏极N^+区域和沟道之间形成电流通路N层。

因此，高耐压MOS FET可理解为在普通MOS FET的漏极端附加了电阻。

功率MOS FET为多个元件在内部并联的结构。

功率MOS FET的结构大致分为两种，一种称为D系列（垂直结构），另一种称为S系列（水平结构）其结构如图1和图2所示。下面对各系列的结构及特点进行更详细的说明。

- D系列（垂直结构）
  在D系列中漏极N^+区域位于硅电路板的下方。栅电极覆盖在沟道之间的整个N層上，以缓和栅极下方的电场集中。电子由源极水平穿过沟道到达N层。此时，栅电极的正电压在N层表面形成了N^+积累层，电子在通过N^+积累层后，垂直穿过整个N层到达漏极。因此，将D系列称为垂直结构，并且外壳为漏极。

  由于保持漏极电压的部分（N层）位于硅中，所以，D系列的单个体积比S系列要小，并且，与相同电压、相同芯片尺寸的S系列相比，D系列的通态电阻更小。

  静电电容具有如图5所示的结电容和MOS电容。

  因为栅极/漏极之间的电容C_{GD}比较大，因此不能忽视C_{GD}对源极接地的输入电容Ciss、输出电容Coss及反馈电容Crss的影响。

  $Ciss=C_{GS}+CGD$

  $Coss=C_{DS}+C_{GD}$

  $Crss=C_{GD}$

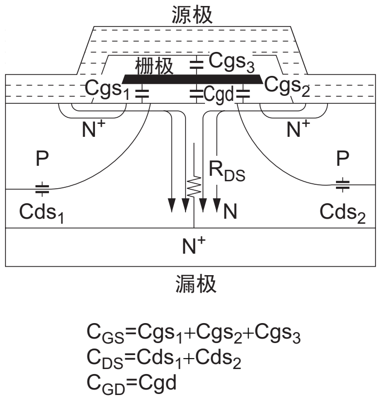

图5 D系列（垂直型）的结构（N沟道）

栅电极采用了在CMOS LSI中具有实际功效的多晶硅。多晶硅的电阻比铝或钼等金属材料高100倍左右，但通过改进多晶硅栅与金属电极的连接后，降低了栅极电阻。在垂直结构中，因为反馈电容Cgd较大，并且漏极电压的依存性较强，所以不能单纯由栅极电阻的时间常数来决定输入电容。这样，关于开关时间的工作分析变得更为复杂。详细内容记载于《功率MOS FET使用时的注意事项》。

- S系列（水平结构）

  在S系列中漏极 N^+ 区域位于硅表面。在漏极 N^+ 区域与沟道之间设置了N层，可使电场强度平均。而且，使源电极扩展到了N层上面，可作为场板来防止栅极附近的电场集中。电子由源极水平穿过沟道及N层到达漏极。因此，将S系列称为水平结构。为了使衬底保持一定的电位，将衬底连接到了源电极，外壳为源极。

  反馈电容Crss对应图6中的Cgd。由于源极场板扩展到了N层上，因此可通过场板与N层的电容Cds来屏蔽Cgd，使得反馈电容Crss的值非常小。

  从芯片及封装两方面来看， S系列的结构适用于输入端与输出端分离的高频产品。

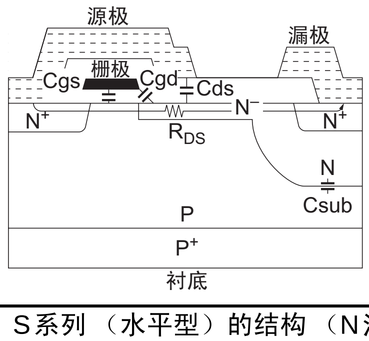

图6 S系列（水平型）的结构（N沟道）

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