

MT02P05N3

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = -20V$
- $I_D = -40A$
- $R_{DS(ON)} = 5.8m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} = 7.5m\Omega @ V_{GS} = -2.5V$

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

Applications

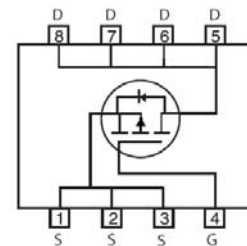
- Notebook Computer
- Portable Battery Pack



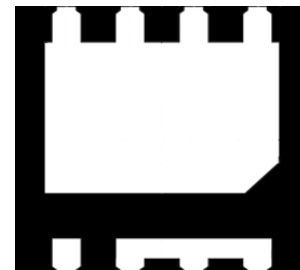
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



DFN3X3-8L

PIN1

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-40	A
Drain Current-Pulsed <small>(Note 1)</small>	I_{DM}	-120	A
Maximum Power Dissipation	P_D	2.6	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <small>(Note 2)</small>	$R_{\theta JA}$	62.5	$^\circ C/W$
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Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT02P05N3	MT02P05N3	DFN3X3-8L	7"	8mm	3000 units

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-	-0.4	-1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-10A$	-	5.8	6.5	m Ω
		$V_{GS}=-2.5V, I_D=-5A$	-	7.5	8.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-3.1A$	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	1020	-	PF
Output Capacitance	C_{oss}		-	110	-	PF
Reverse Transfer Capacitance	C_{rss}		-	90	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=2\Omega$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	10.5	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	51	-	nS
Turn-Off Fall Time	t_f		-	28	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-4.5A,$ $V_{GS}=-10V$	-	11.6	-	nS
Gate-Source Charge	Q_{gs}		-	3.5	-	nS
Gate-Drain Charge	Q_{gd}		-	5.9	-	nS
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-1A$	-	-0.7	-1.3	V
Diode Forward Current (Note 2)	I_S		-	-	-2.3	A

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Characteristics Curve ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

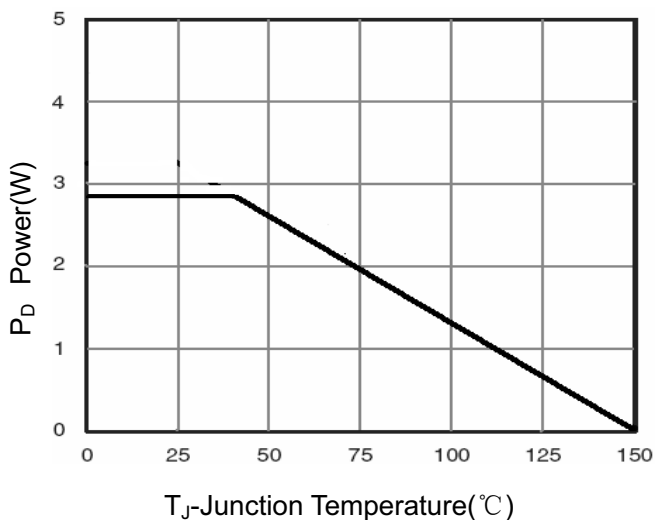


Figure 1 Power Dissipation

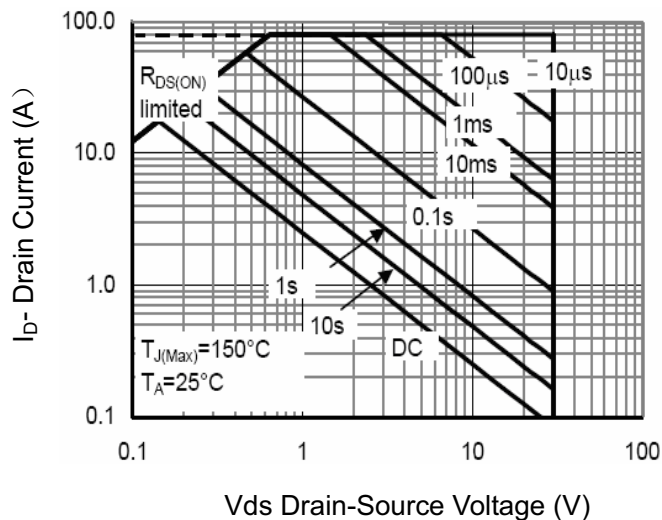


Figure 2 Safe Operation Area

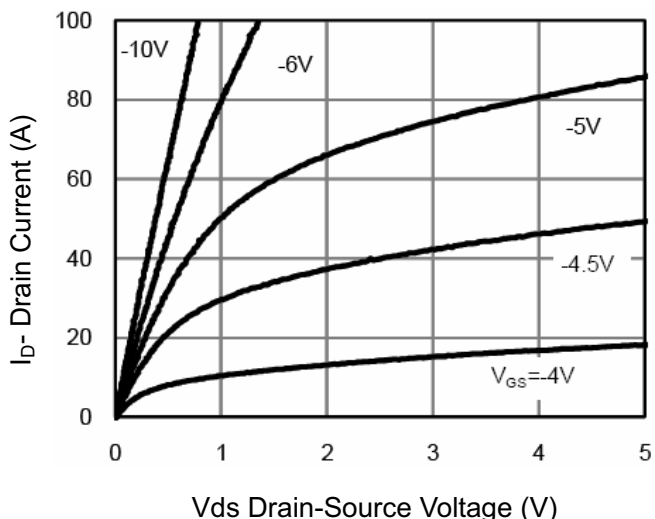


Figure 3 Output Characteristics

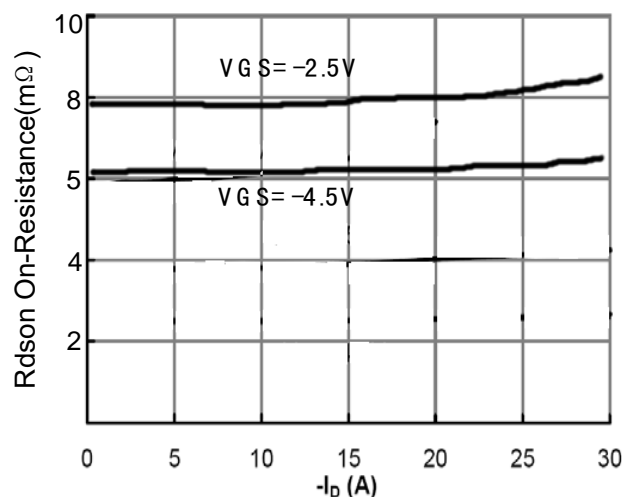


Figure 4 Drain-Source On-Resistance

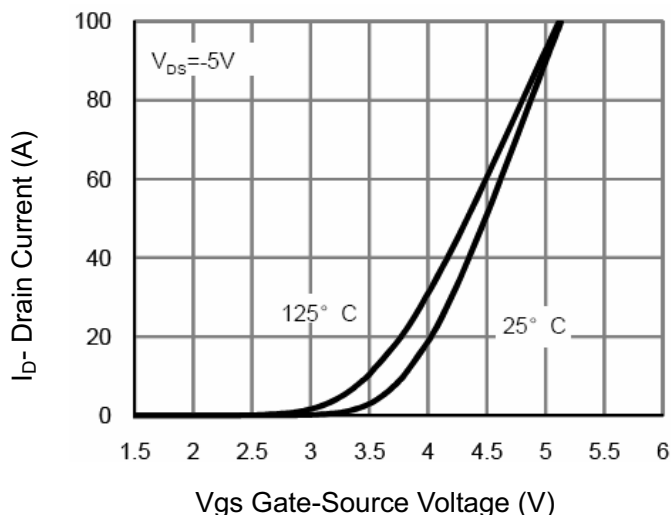


Figure 5 Transfer Characteristics

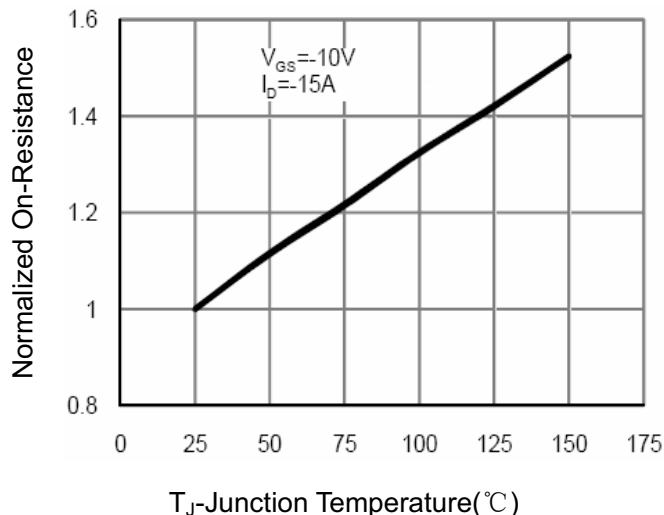
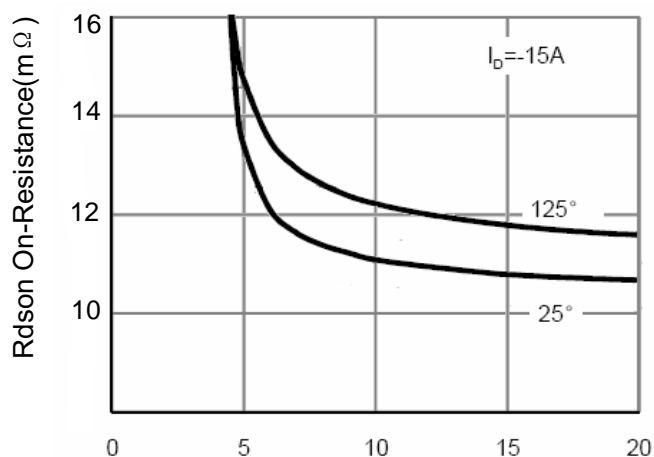
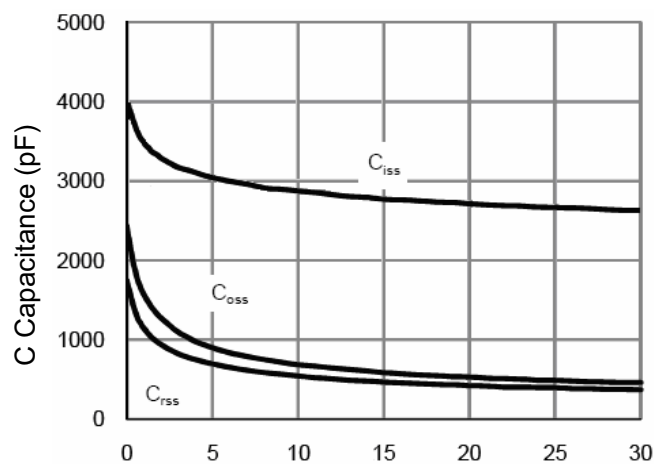


Figure 6 Drain-Source On-Resistance

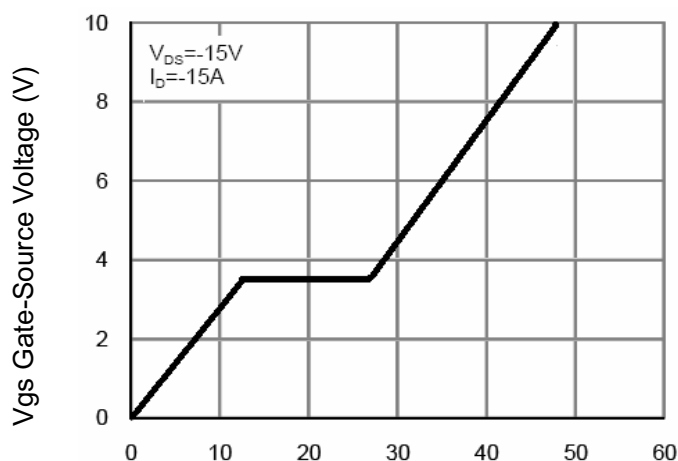
Characteristics Curve ($T_A=25^{\circ}\text{C}$, unless otherwise noted)



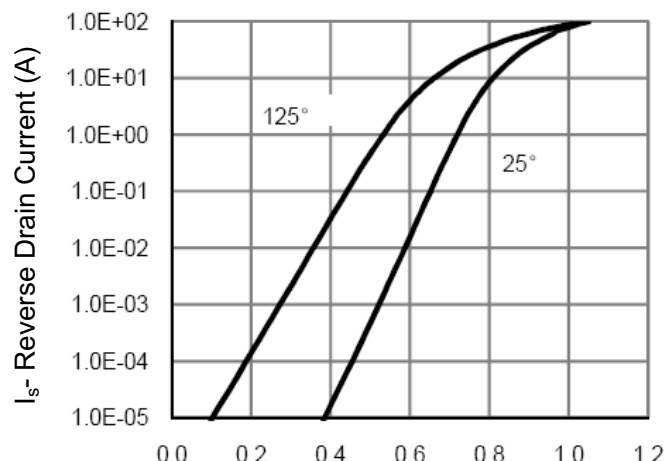
Vgs Gate-Source Voltage (V)
Figure 7 Rdson vs Vgs



Vds Drain-Source Voltage (V)
Figure 8 Capacitance vs Vds



Qg Gate Charge (nC)
Figure 9 Gate Charge



Vsd Source-Drain Voltage (V)
Figure 10 Source-Drain Diode Forward

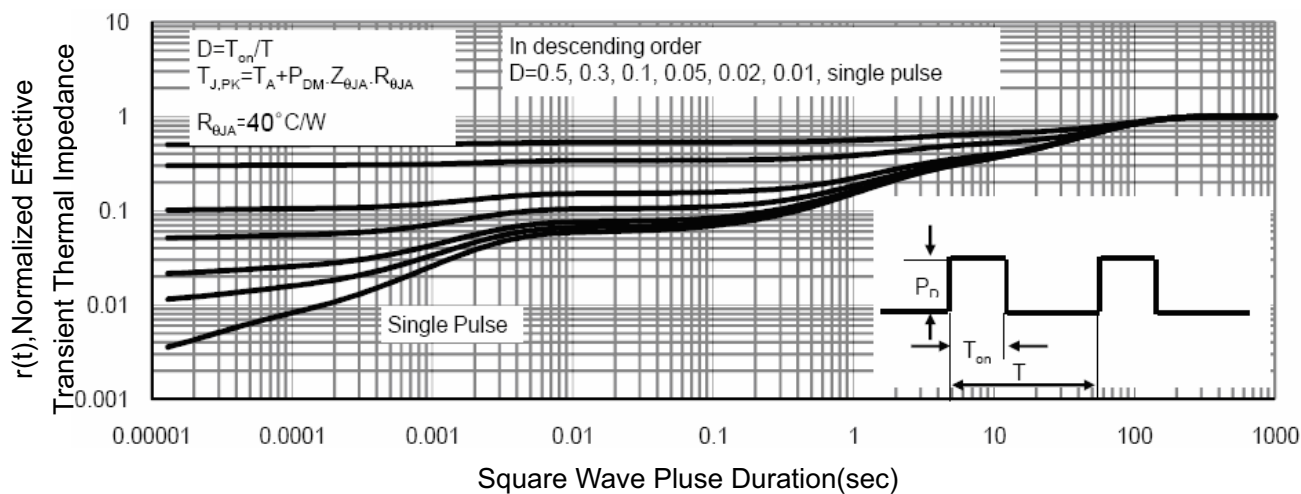
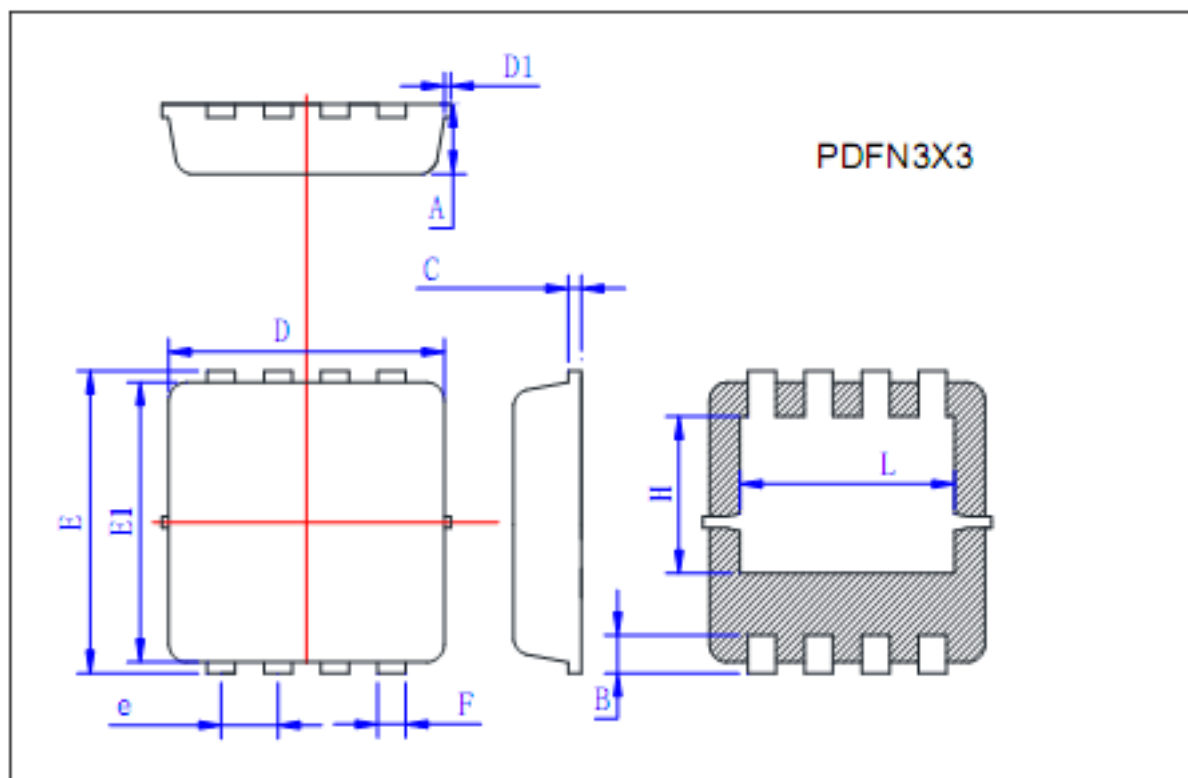


Figure 11 Normalized Maximum Transient Thermal Impedance

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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