

MT100P50S

-100V/-30A P-Channel Advanced Power MOSFET

V_{DS}	-100	V
$R_{DS(on),TYP} @ V_{GS}=-10V$	46	m Ω
$R_{DS(on),TYP} @ V_{GS}=-4.5V$	48	m Ω
I_D	-30	A

Features

- P-Channel, -5V Logic Level Control
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant



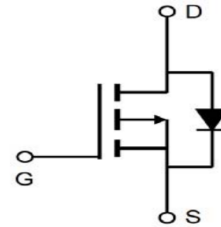
Halogen-Free



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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Maximum ratings, at $T_J = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-100	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$ -30	A
I_D	Continuous drain current @ $V_{GS} = -10V$	$T_C = 25^\circ\text{C}$ -30	A
		$T_C = 100^\circ\text{C}$ -25	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ -95	A
EAS	Avalanche energy, single pulsed ②	235	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$ 101	W
V_{GS}	Gate-Source voltage	± 20	V
$T_{STG} T_J$	Storage and operating temperature range	-55 to 175	$^\circ\text{C}$
Thermal Characteristics			
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	100	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-100V, V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-100V, V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.7	-2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =-10V, I _D =-10 A	--	46	60	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =-4.5V, I _D =-8A	--	48	70	mΩ
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-25V, V _{GS} =0V, f=1MHz	--	3300	--	pF
C _{oss}	Output Capacitance		--	93	--	pF
C _{rss}	Reverse Transfer Capacitance		--	39	--	pF
Q _g	Total Gate Charge	V _{DS} =-50V, I _D =-2A, V _{GS} =-10V	--	76	--	nC
Q _{gs}	Gate-Source Charge		--	7.4	--	nC
Q _{gd}	Gate-Drain Charge		--	16	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-50V, I _D =-2A, R _G =9.1Ω, V _{GS} =-10V	--	5	--	nS
t _r	Turn-on Rise Time		--	31	--	nS
t _{d(off)}	Turn-Off Delay Time		--	16	--	nS
t _f	Turn-Off Fall Time		--	22	--	nS
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-2A, V _{GS} =0V	--	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C, I _{sd} =-2A, V _{GS} =0V	--	35	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=-100A/μs		55		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -7A, V_{GS} = -10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycles ≤ 2%.

Typical Electrical And Thermal Characteristics (Curves)

Figure 1. Output Characteristics

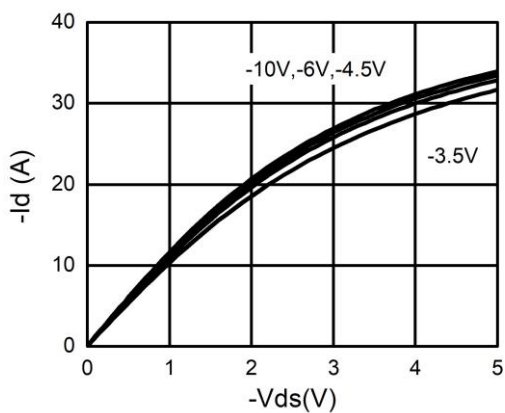


Figure 2. Transfer Characteristics

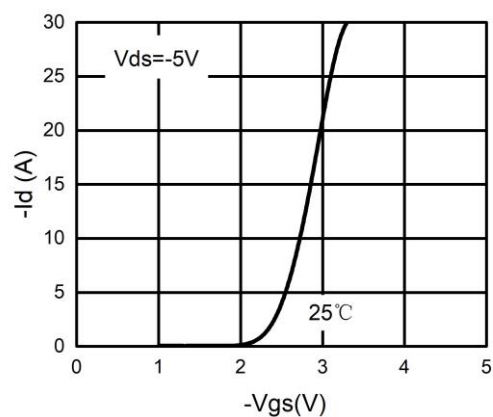


Figure 3. Power Dissipation

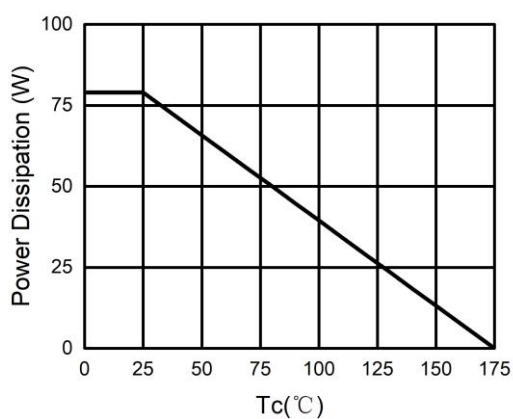


Figure 4. Drain Current

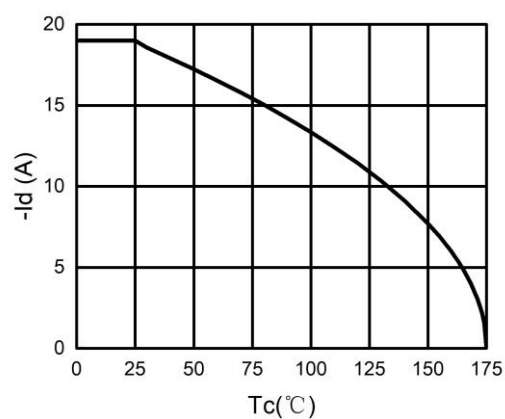
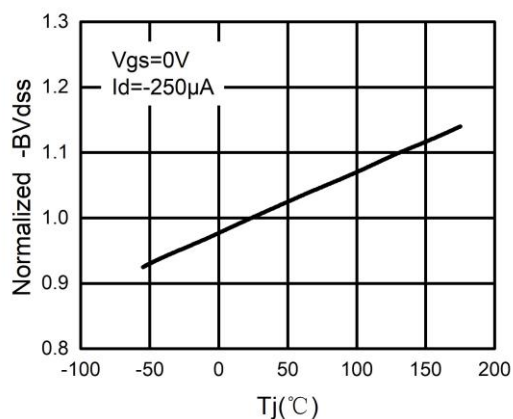
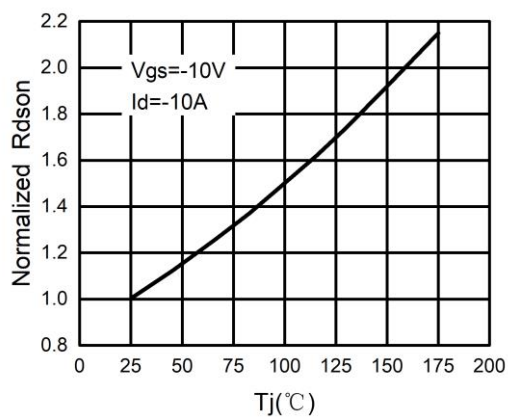
Figure 5. BV_{DSS} vs Junction TemperatureFigure 6. $R_{DS(ON)}$ vs Junction Temperature

Figure 7. Gate Charge Waveforms

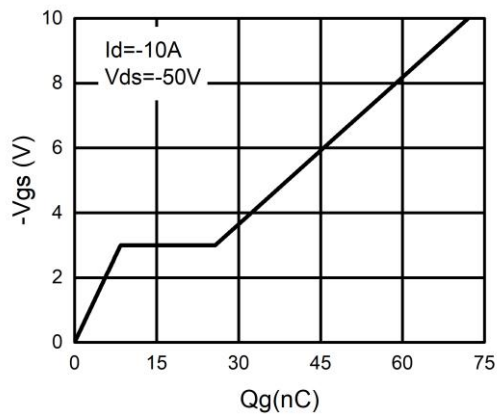


Figure 8. Capacitance

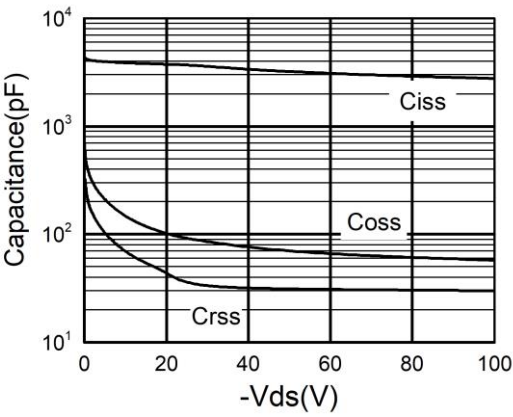


Figure 9. Body-Diode Characteristics

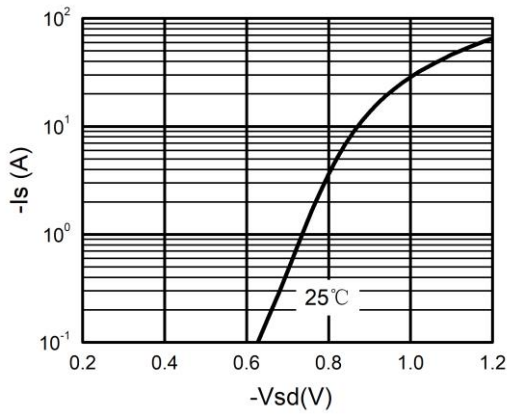
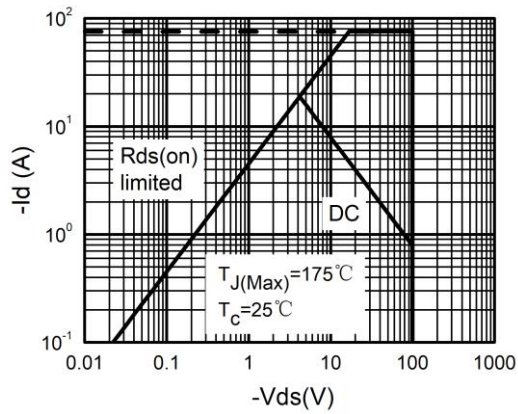
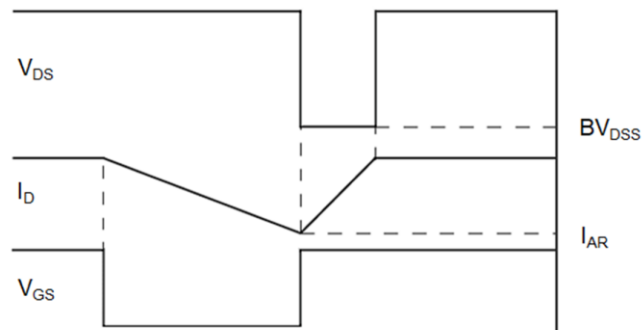
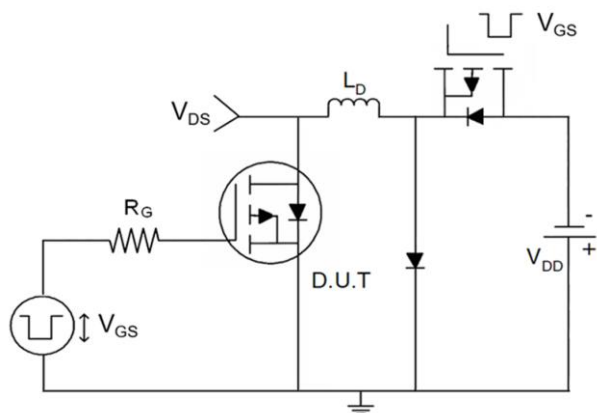


Figure 10. Maximum Safe Operating Area

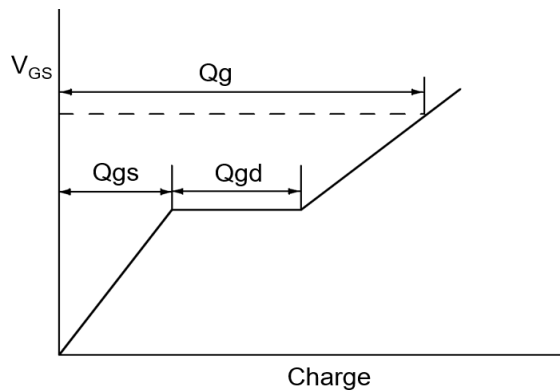
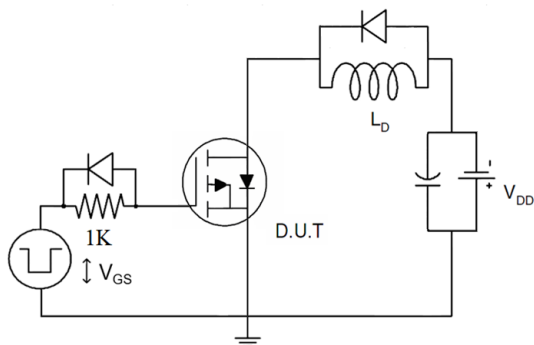


Test Circuit

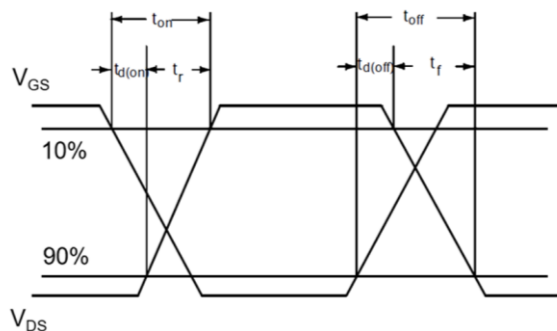
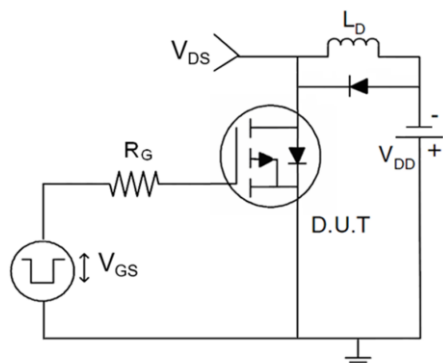
1) E_{AS} Test Circuits



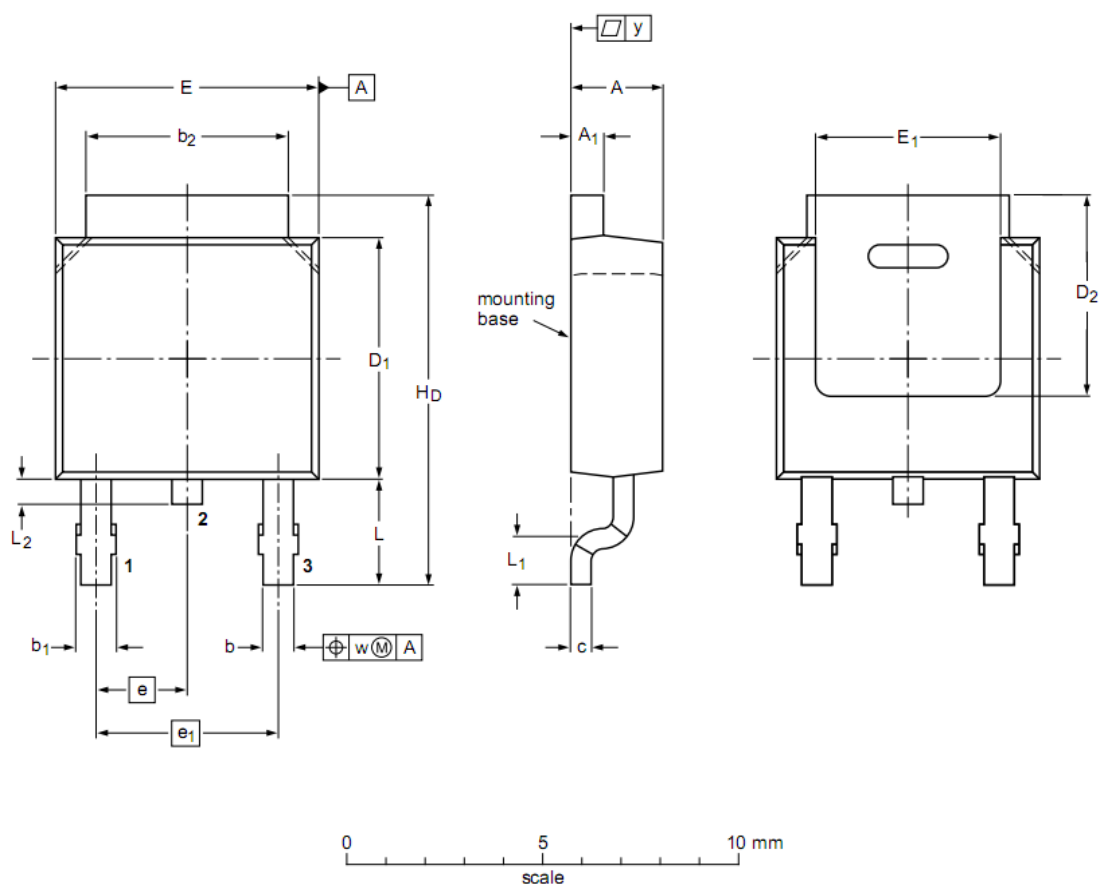
2) Gate Charge Test Circuit



3) Switch Time Test Circuit



TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A ₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b ₁	0.77	0.85	1.14
b ₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D ₁	5.98	6.10	6.223
D ₂	5.21	--	--
E	6.40	6.60	6.731
E ₁	4.40	--	--
e	2.286 BSC		
e ₁	--	4.57	--
H _D	9.40	10.00	10.40
L	2.743 REF		
L ₁	1.40	1.52	1.77
L ₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

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