

# MT10G020T

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS} = 100V$
- $I_D = 300A$
- $R_{DS(ON)} = 1.7 m\Omega @ V_{GS} = 10V$

### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.
- TOLL Package

### Applications

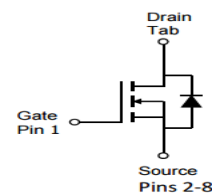
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



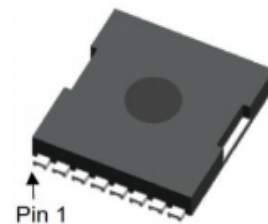
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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter		Steady State	Units
V <sub>DS</sub>	Drain-Source Voltage		100	V
V <sub>GS</sub>	Gate-Source Voltage		± 20	V
I <sub>D</sub>	Continuous Drain Current <sup>1</sup>	T <sub>C</sub> = 25°C	300	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>		1190	A
I <sub>S</sub>	Continuous Source Current (Diode Conduction) <sup>1</sup>		280	A
E <sub>AS</sub>	Single Pulse Drain-Source Avalanche Energy <sup>3</sup>		735	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> = 25°C	330	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range		-55~150	°C

Notes:

1. Surface Mounted on 1" x 1" FR4 Board,  $t \leq 10$  Sec.
2. Pulse width limited by maximum junction temperature.
3. The test condition is  $T_J = 25^\circ C$ ,  $V_{DD} = 30V$ ,  $V_{GS} = 10V$ ,  $L = 0.1mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 50A$ .

## Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.4	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

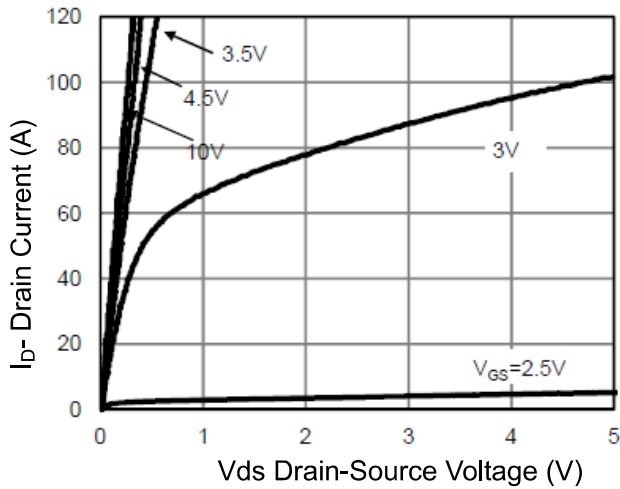
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	100	nA
On Characteristics						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	2.8	5.0	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	1.7	2.6	mΩ
Dynamic Characteristics <sup>b</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1.0MHz	-	10123	-	PF
Output Capacitance	C <sub>OSS</sub>		-	2049	-	PF
Reverse Transfer Capacitance	C <sub>rSS</sub>		-	77	-	PF
Switching Characteristics						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50V, I <sub>D</sub> =90A V <sub>GS</sub> =10V, R <sub>G</sub> =3.0Ω	-	30	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	105	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	81	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	109	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> =90A , V <sub>GS</sub> =10V	-	140		nC
Gate-Source Charge	Q <sub>gs</sub>		-	48		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	30		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	0.75	1.4	V
Diode Forward Current	I <sub>S</sub>		-	-	300	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 90A di/dt = 500A/μs	-	56	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	96	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Note:

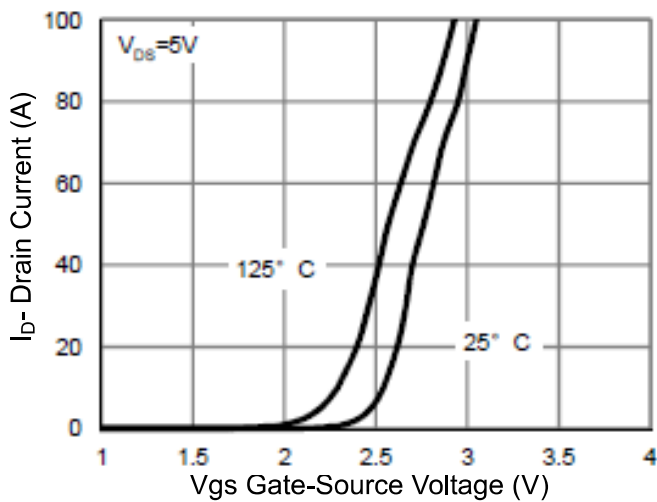
a. Pulse test; pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

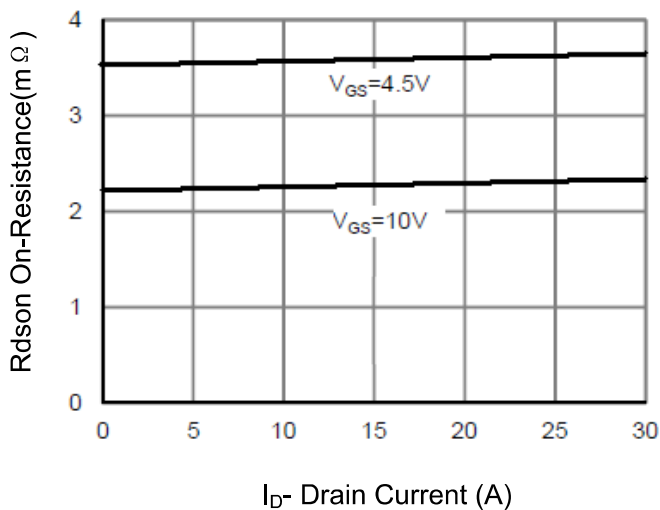
### Typical Electrical and Thermal Characteristics (Curves)



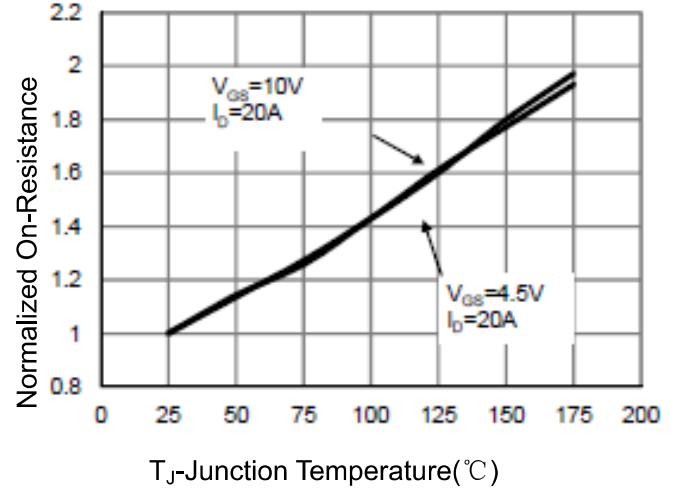
**Figure 1 Output Characteristics**



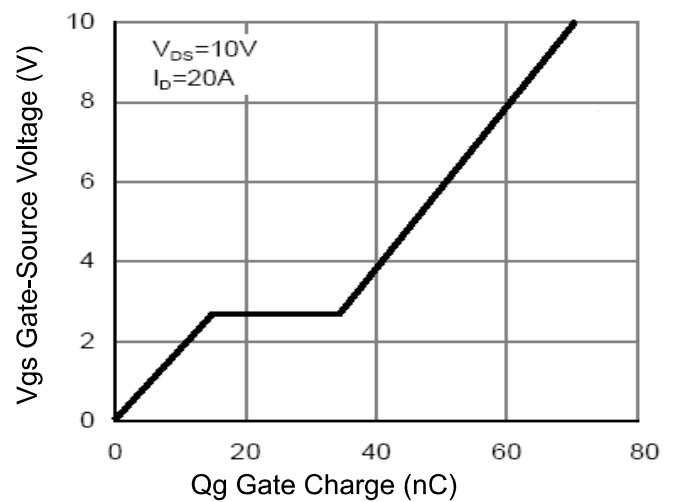
**Figure 2 Transfer Characteristics**



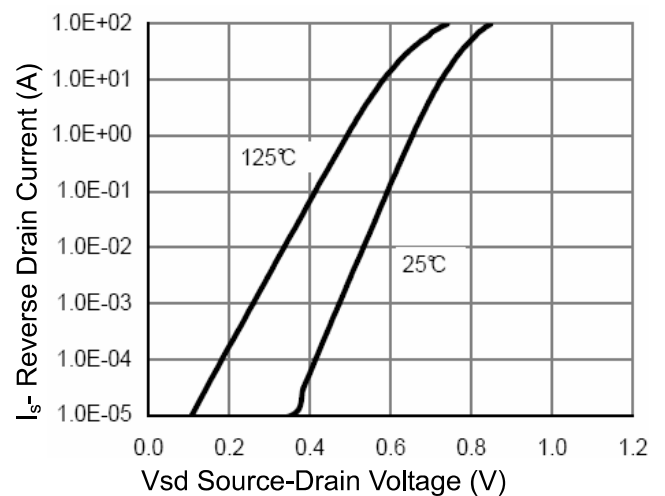
**Figure 3  $R_{DS(on)}$  - Drain Current**



**Figure 4  $R_{DS(on)}$  - Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source-Drain Diode Forward**

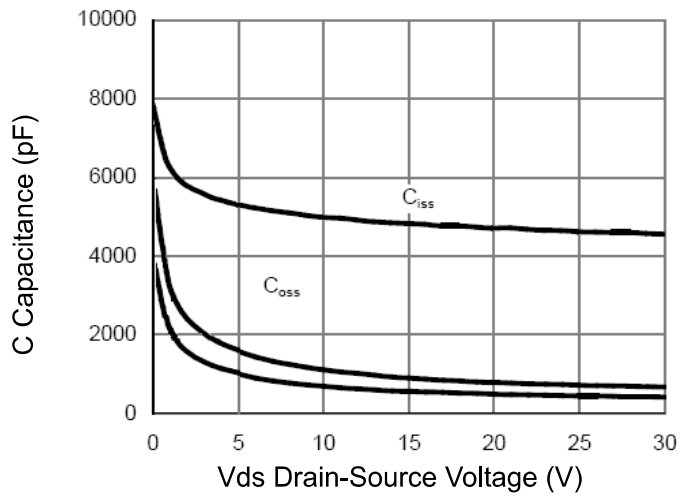


Figure 7 Capacitance vs Vds

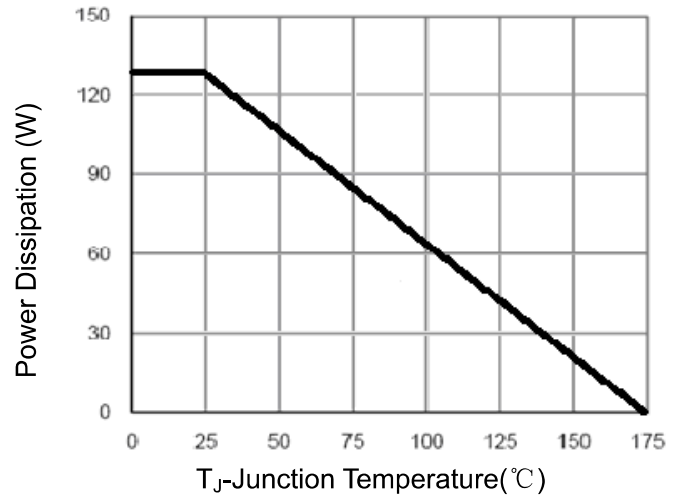


Figure 9 Power De-rating

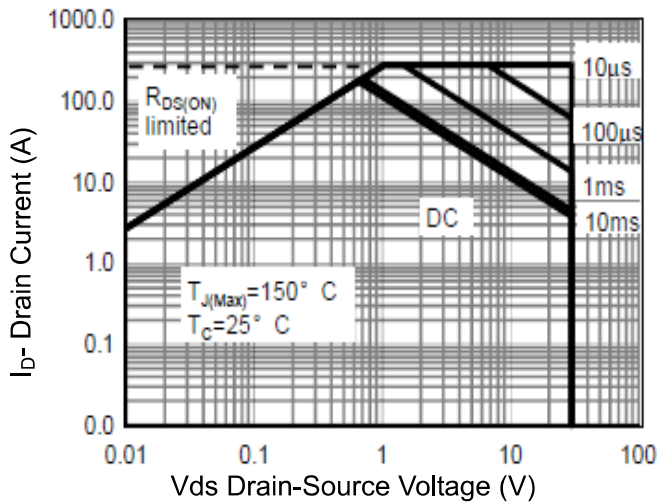


Figure 8 Safe Operation Area

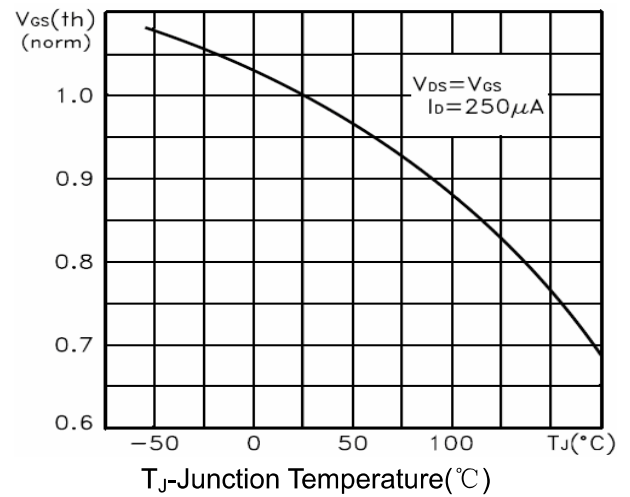
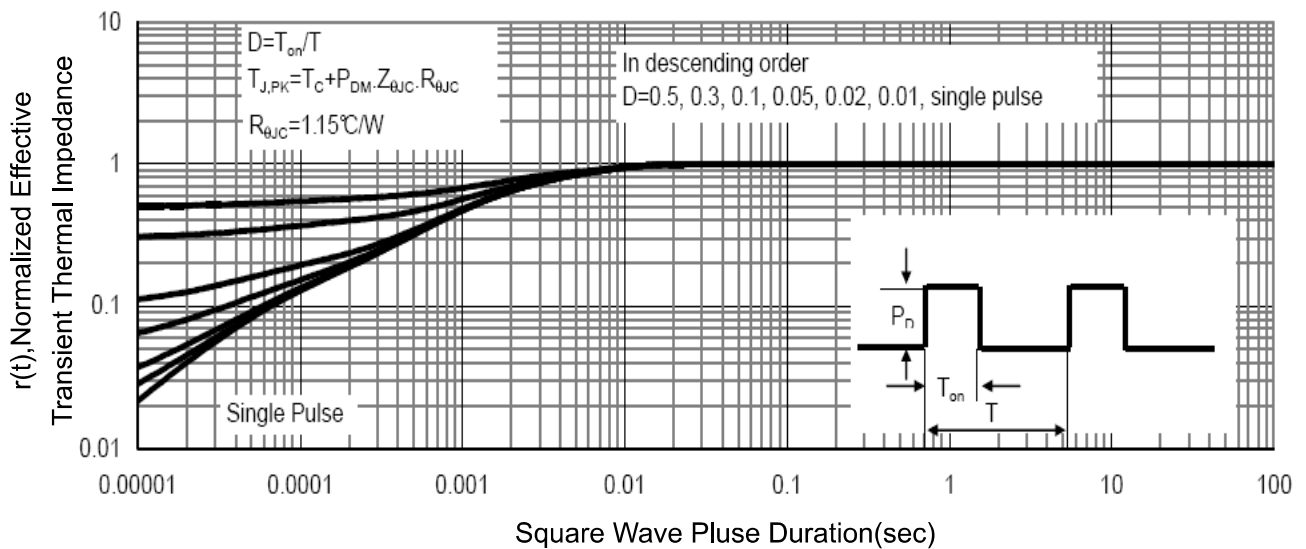
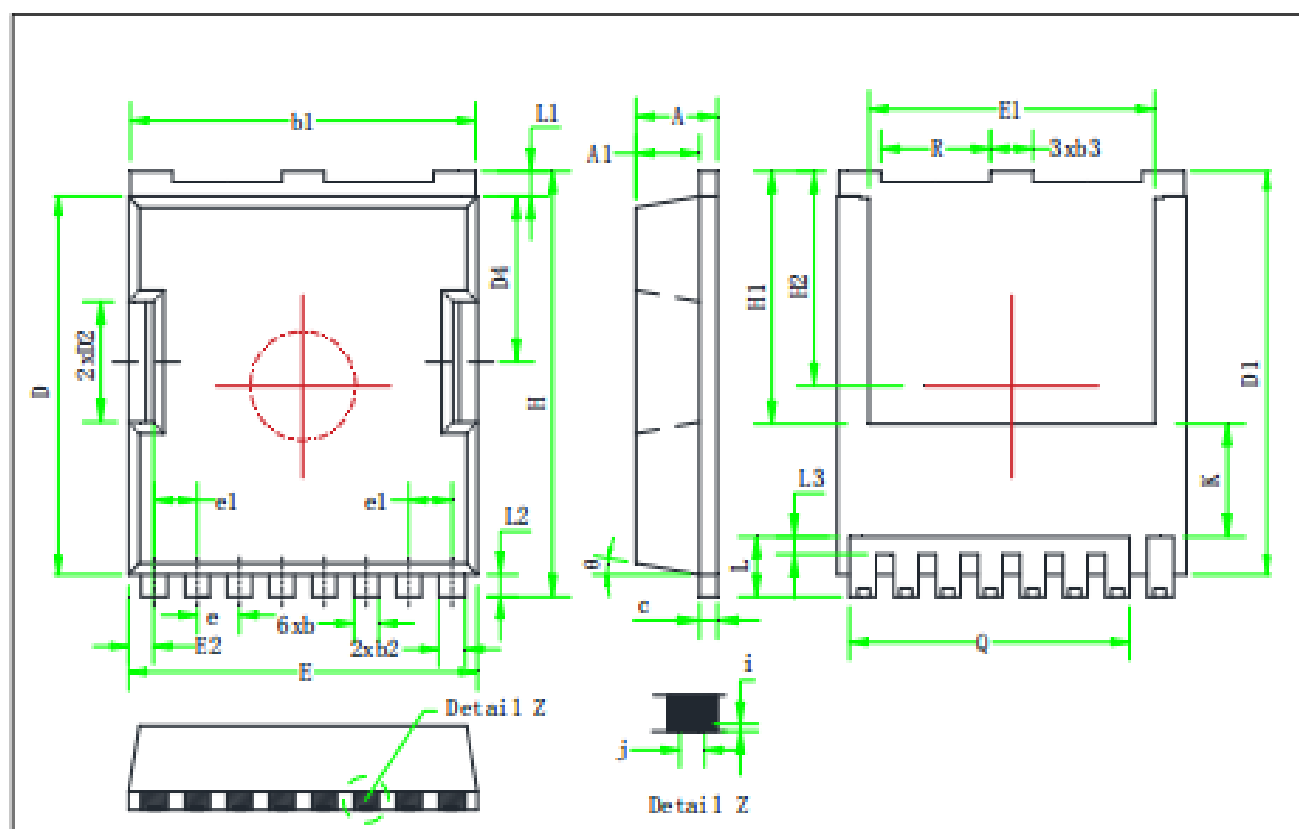
Figure 10  $V_{GS(th)}$  vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

## Package Mechanical Data(TOLL)



Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	2.25	2.30	2.35	E2	0.65	0.70	0.75
A1	1.75	1.80	1.85	H	11.60	11.70	11.80
b	0.65	0.70	0.75	H1	6.95 BSC		
b1	9.75	9.80	9.85	H2	5.90 BSC		
b2	0.70	0.75	0.80	i	0.10 REF		
b3	1.15	1.20	1.25	j	0.35 REF		
c	0.45	0.50	0.55	K	3.10 REF		
D	10.35	10.40	10.45	L	1.55	1.65	1.75
D1	11.00	11.10	11.20	L1	0.65	0.70	0.75
D2	3.25	3.30	3.35	L2	0.50	0.60	0.70
D4	4.50	4.55	4.60	L3	0.40	0.50	0.60
e	1.20 BSC			Q	7.95 REF		
e1	1.225 BSC			R	3.05	3.10	3.15
E	9.85	9.90	9.95	θ	10°REF		
E1	8.00	8.10	8.20				

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