

# MT10G10

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS} = 100V$
- $I_D = 15A$  ( $V_{GS} = 10V$ )
- $R_{DS(ON)} < 13\text{ m}\Omega$  @  $V_{GS} = 10V$

The MT10G10 uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- Pb-free lead plating

### Application

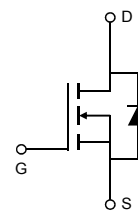
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



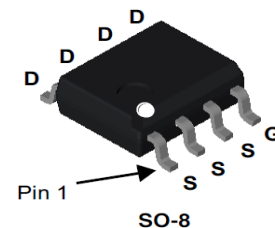
**MT Semiconductor®**

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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT10G10	MT10G10	SO-8	330mm	120mm	2500 units

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous (Package Limited)	$I_D$	15	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D (100^\circ\text{C})$	9	A
Pulsed Drain Current	$I_{DM}$	25	A
Maximum Power Dissipation	$P_D$	2.8	W
Derating factor		0.84	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	198	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

**Thermal Characteristic**

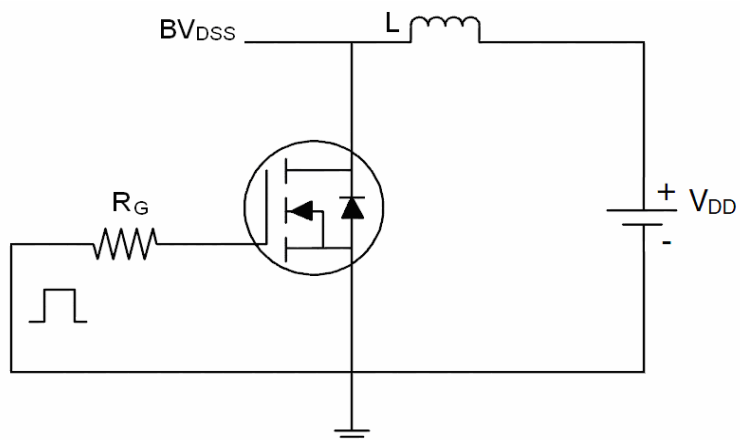
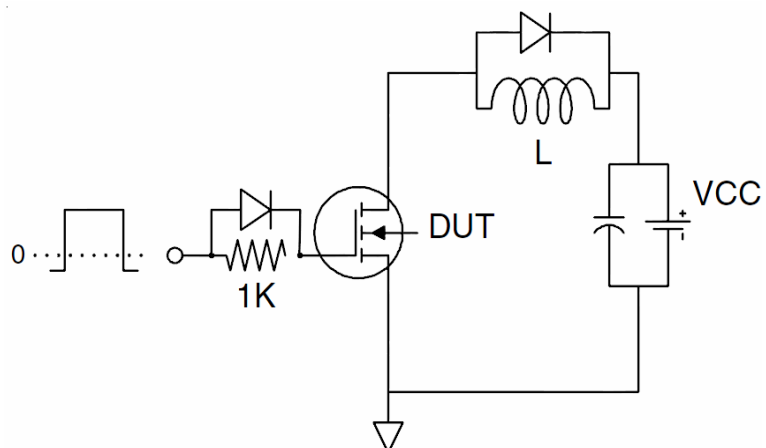
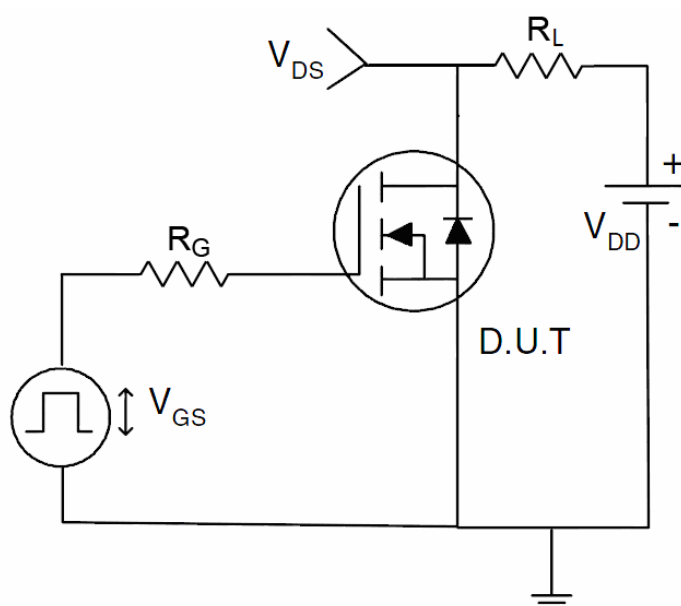
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	25	$^{\circ}\text{C/W}$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

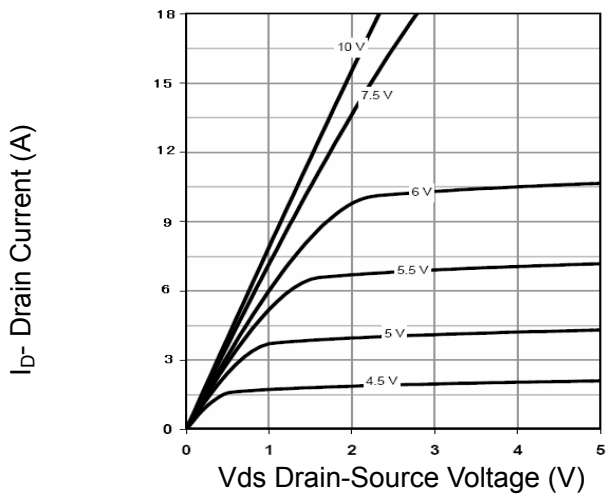
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V\ I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5	2	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	-	10	13	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=5A$	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	1600	-	PF
Output Capacitance	$C_{oss}$		-	100	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	29	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=5A$ $V_{GS}=10V, R_G=4.7\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	45	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	31	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=5A,$ $V_{GS}=10V$	-	48		nC
Gate-Source Charge	$Q_{gs}$		-	15		nC
Gate-Drain Charge	$Q_{gd}$		-	8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=5A$	-		1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	5	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ (Note3)	-	55		nS
Reverse Recovery Charge	$Q_{rr}$		-	93		nC

**Notes:**

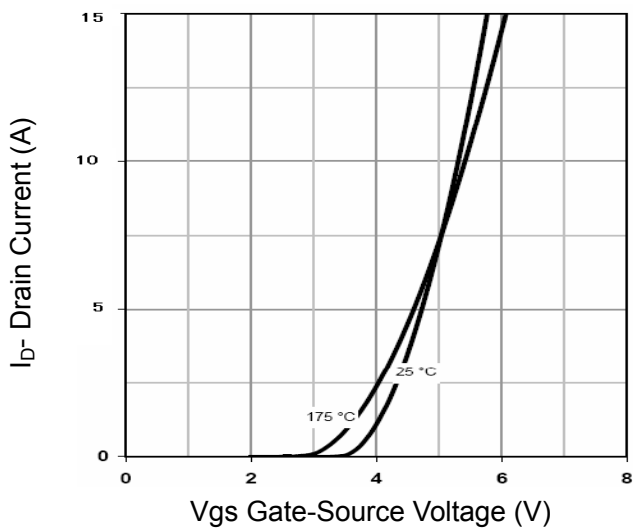
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25\Omega$

**Test Circuit****1)  $E_{AS}$  test Circuit****2) Gate charge test Circuit****3) Switch Time Test Circuit**

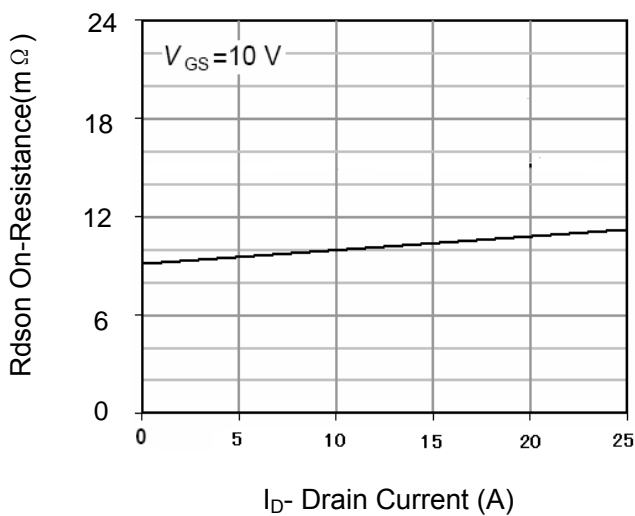
## Typical Electrical and Thermal Characteristics



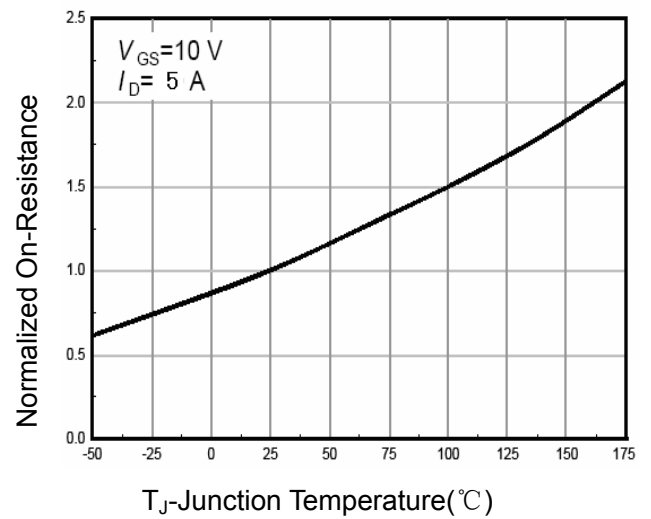
**Figure 1 Output Characteristics**



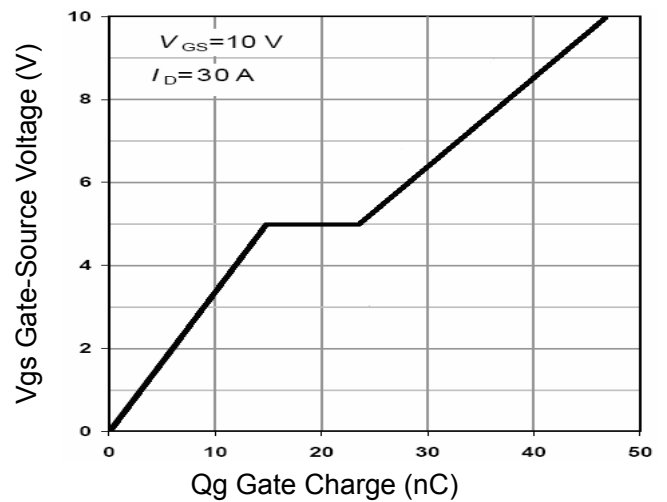
**Figure 2 Transfer Characteristics**



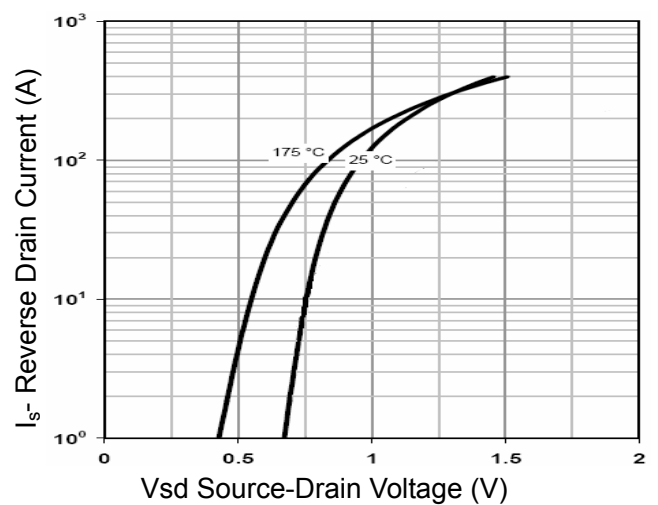
**Figure 3  $R_{DS(on)}$ - Drain Current**



**Figure 4  $R_{DS(on)}$ -Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

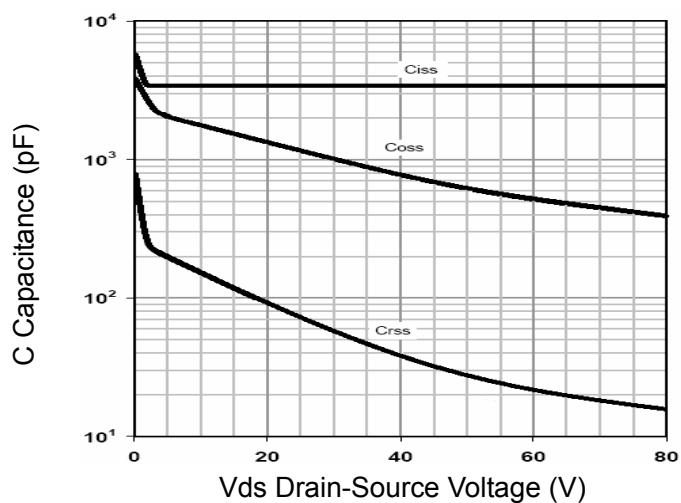
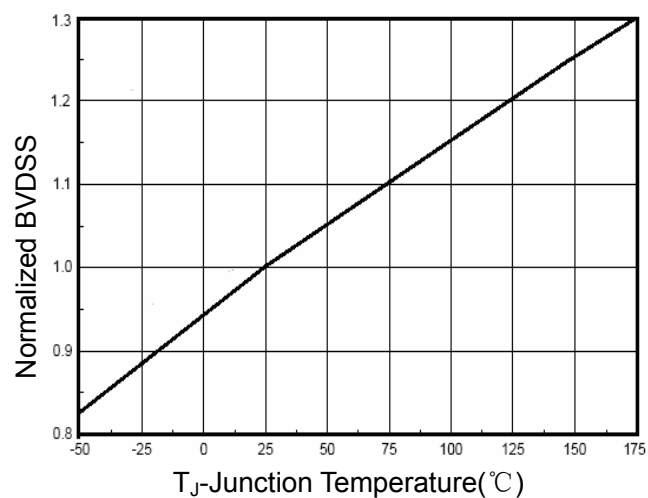
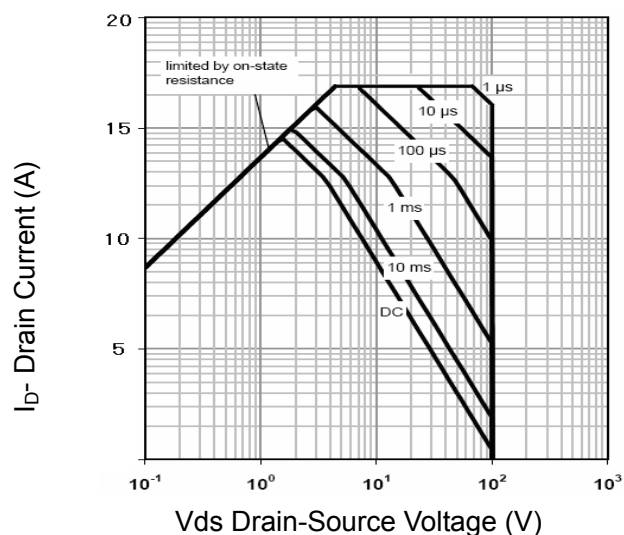
Figure 7 Capacitance vs  $V_{ds}$ Figure 9  $BV_{DSS}$  vs Junction Temperature

Figure 8 Safe Operation Area

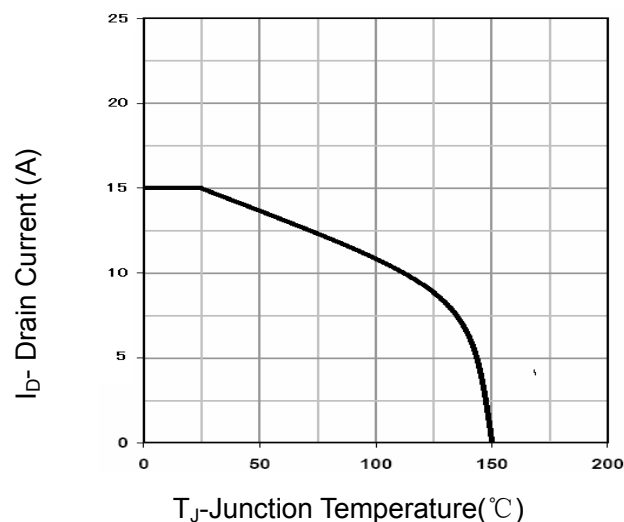


Figure 10 Current De-rating

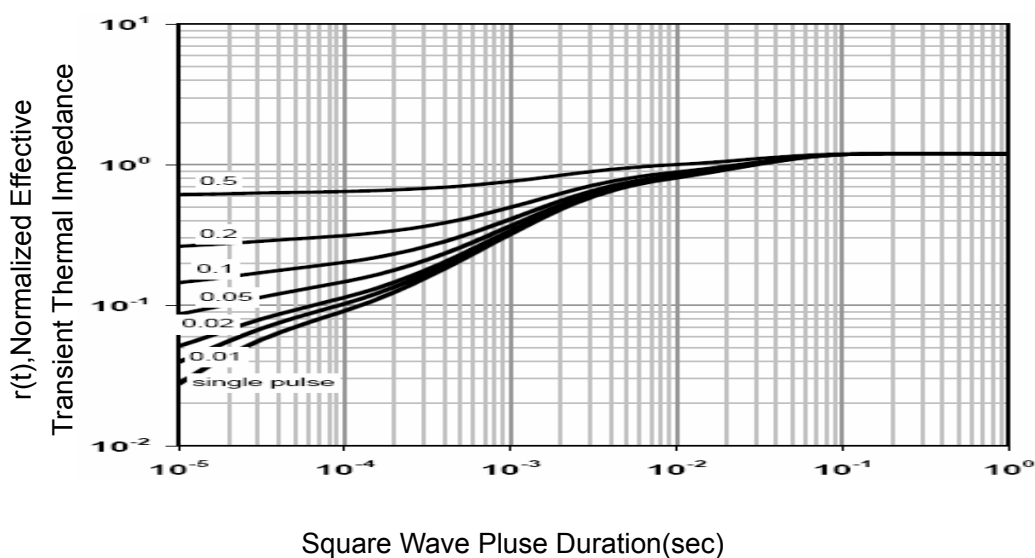
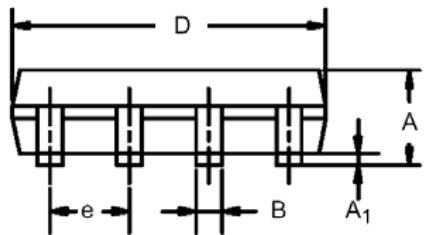
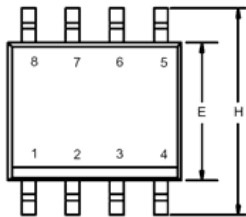


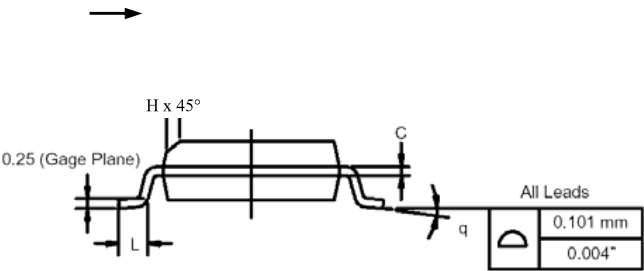
Figure 11 Normalized Maximum Transient Thermal Impedance

Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°



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