

# MT19N20

## N-Channel 200V Power MOSFET

### Features

- Typ  $R_{DS(on)}=480m\Omega @ V_{GS}=10V, I_D=2A$
- Fast Switching Speed
- Low Gate Charge
- High Power and Current Handling Capability

### General Description

This N-Channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

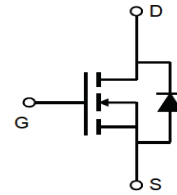
- Power Switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



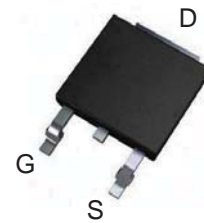
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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



TO-252-2L

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	5	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	10	A
Maximum Power Dissipation	$P_D$	35	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	3.5	$^\circ\text{C/W}$
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### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT19N20	MT19N20	TO-252-2L	-	-	2500

**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	200	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A	-	480	580	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =2A	-	8	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	580	-	PF
Output Capacitance	C <sub>OSS</sub>		-	90	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	3	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =100V, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	10	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	12	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =100V, I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	12	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.8	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =2A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	2	A

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

### Typical Electrical and Thermal Characteristics (Curves)

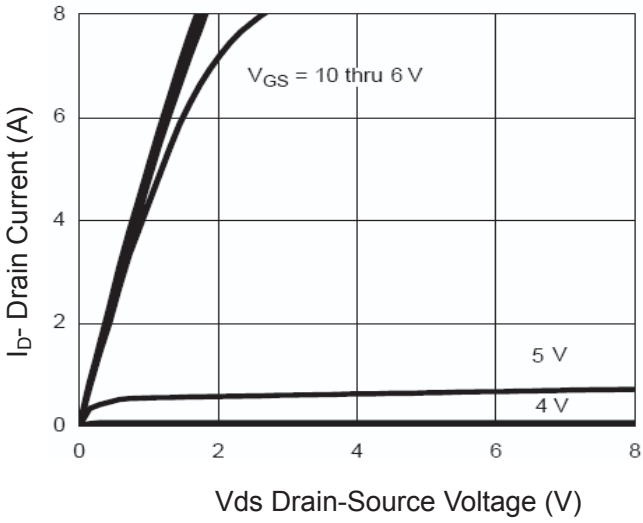


Figure 1 Output Characteristics

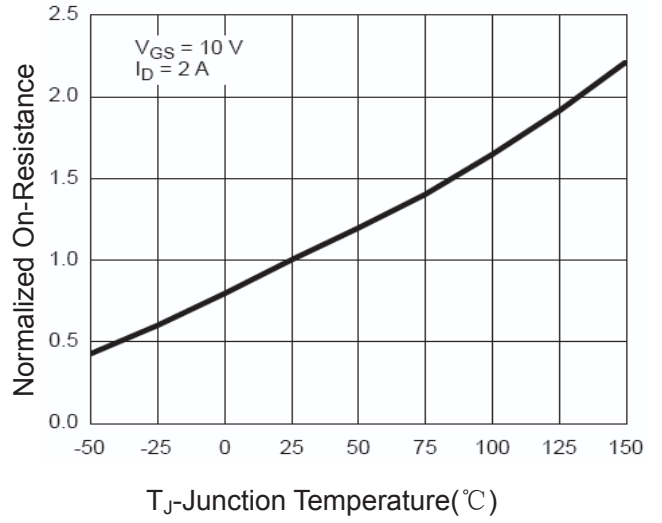


Figure 4  $R_{dson}$ -Junction Temperature

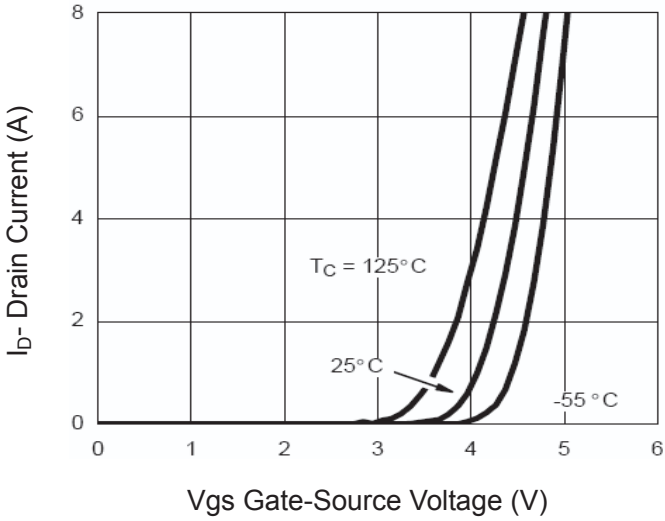


Figure 2 Transfer Characteristics

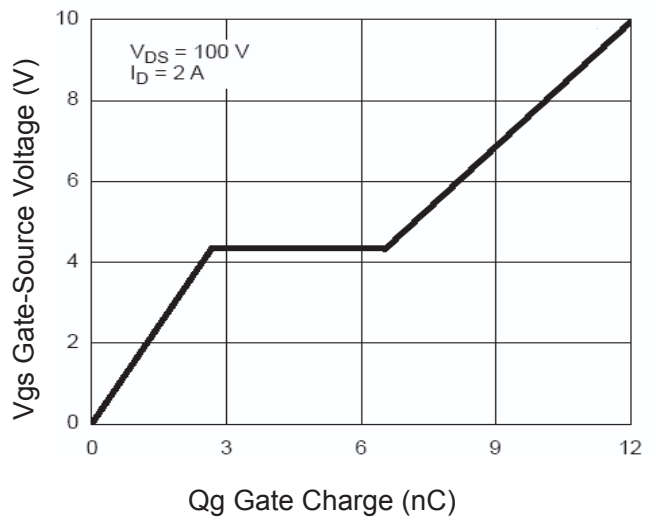


Figure 5 Gate Charge

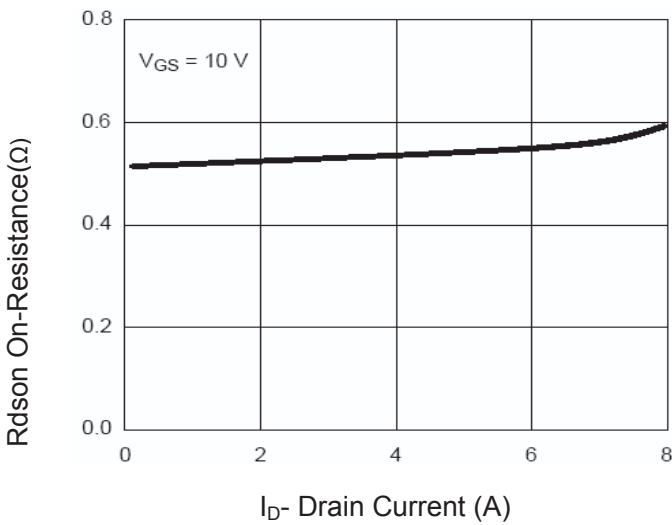


Figure 3  $R_{dson}$ - Drain Current

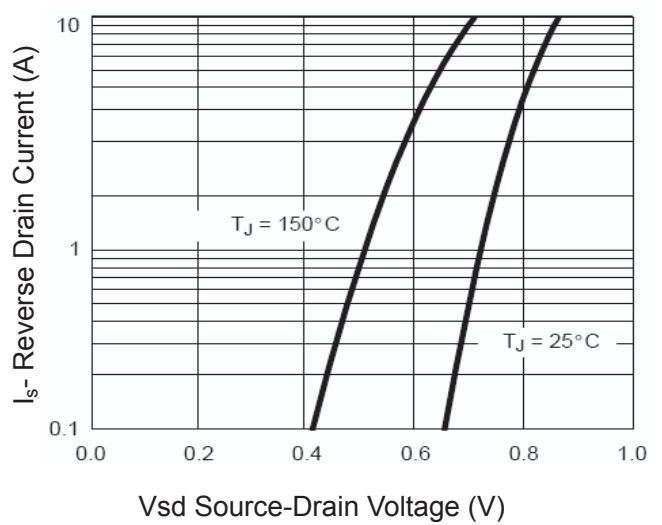


Figure 6 Source- Drain Diode Forward

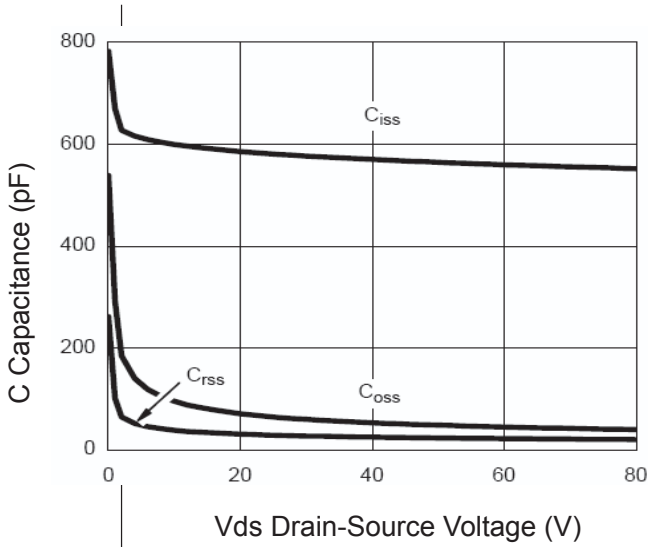


Figure 7 Capacitance vs Vds

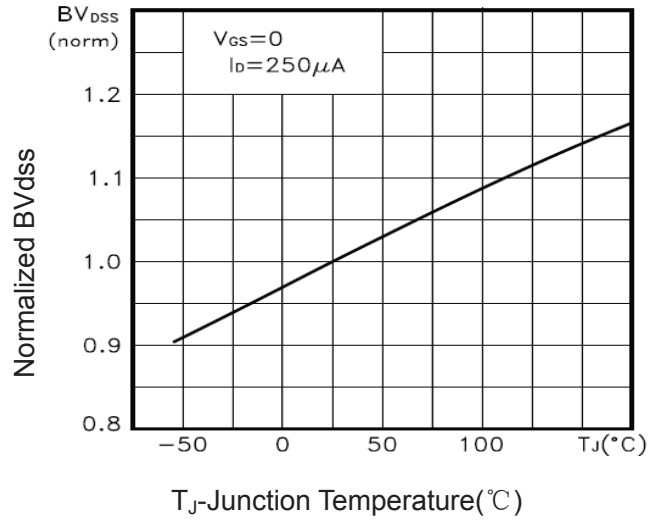


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

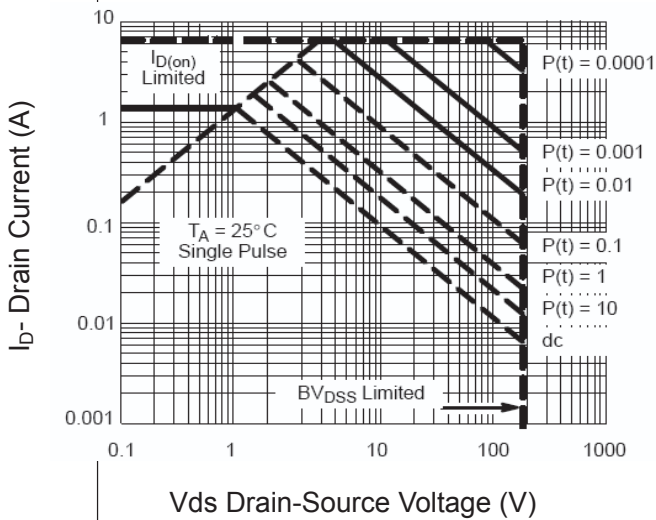


Figure 8 Safe Operation Area

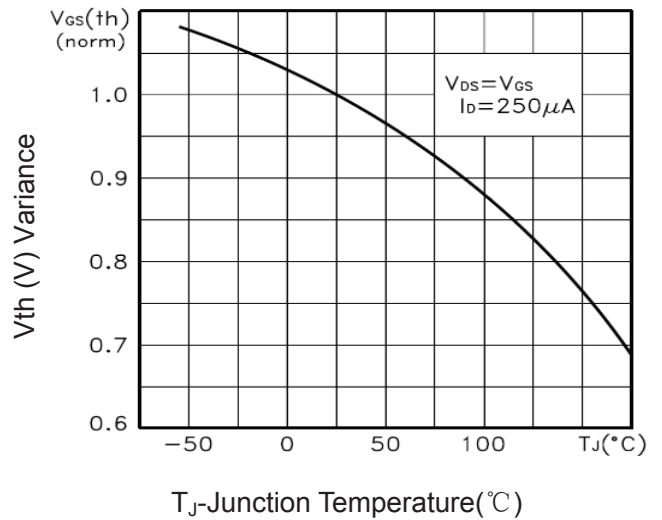


Figure 10 V<sub>GS(th)</sub> vs Junction Temperature

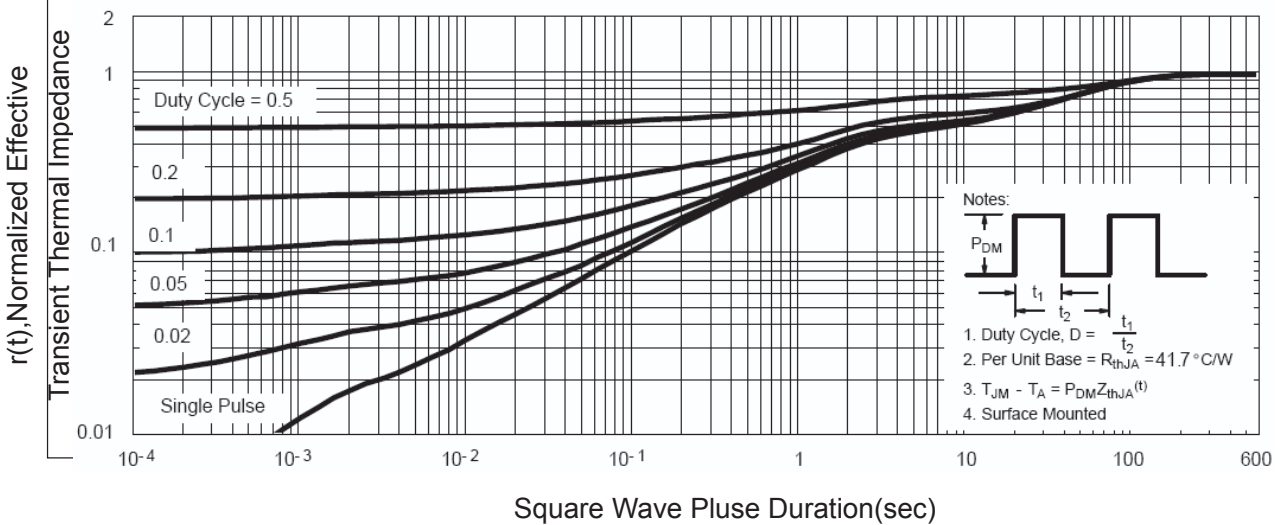
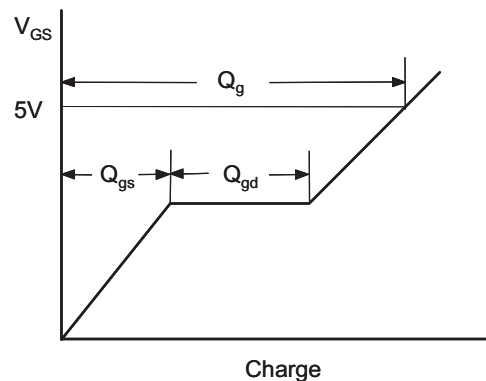
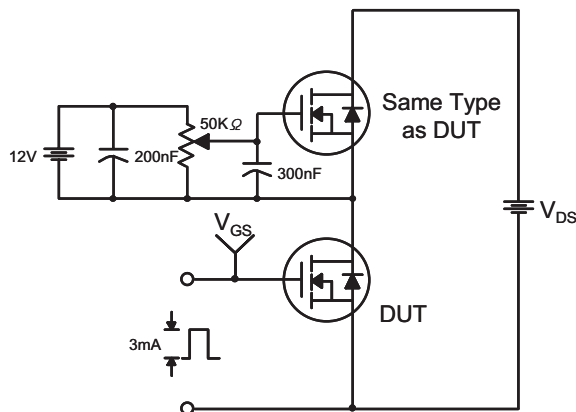
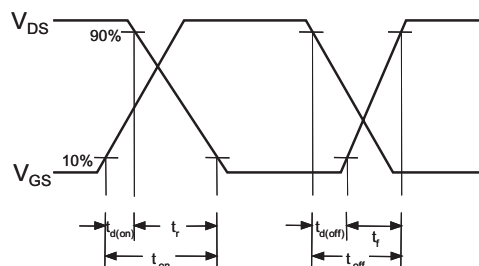
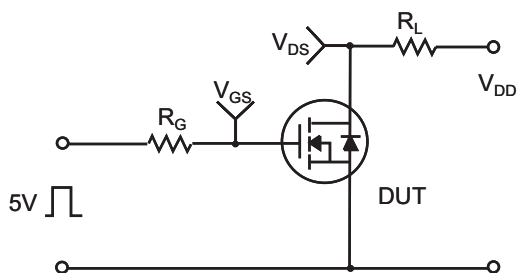


Figure 11 Normalized Maximum Transient Thermal Impedance

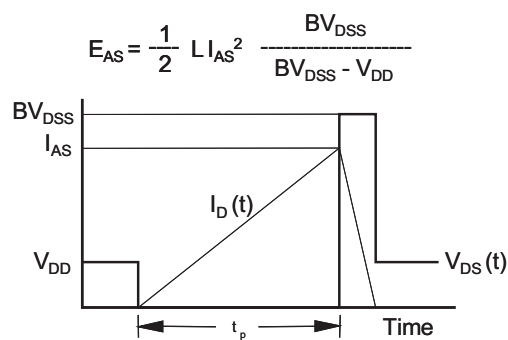
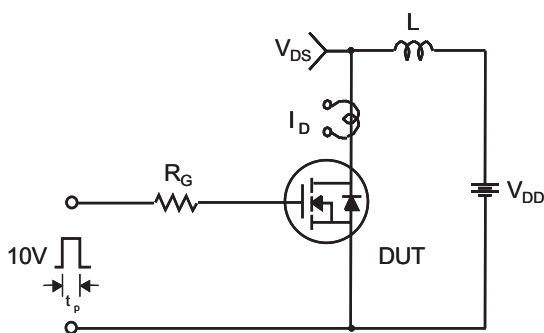
**Gate Charge Test Circuit & Waveform**



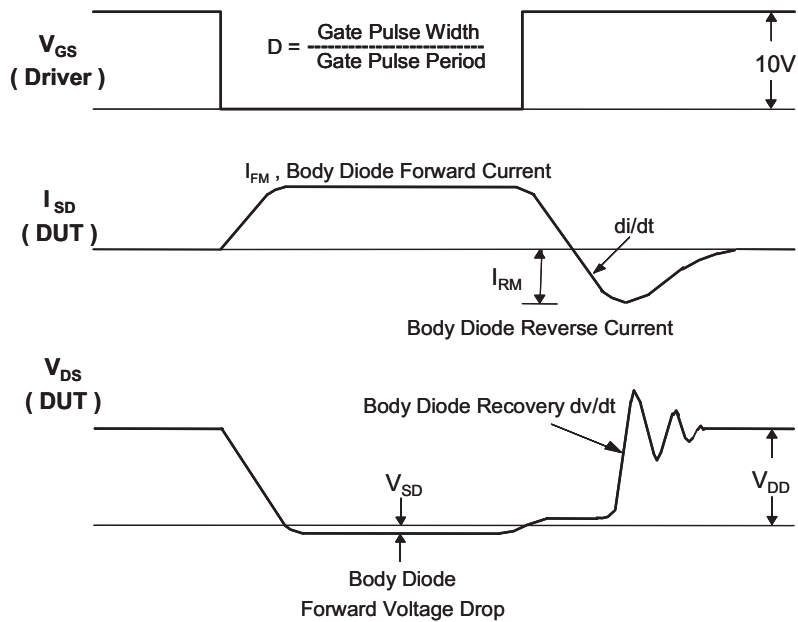
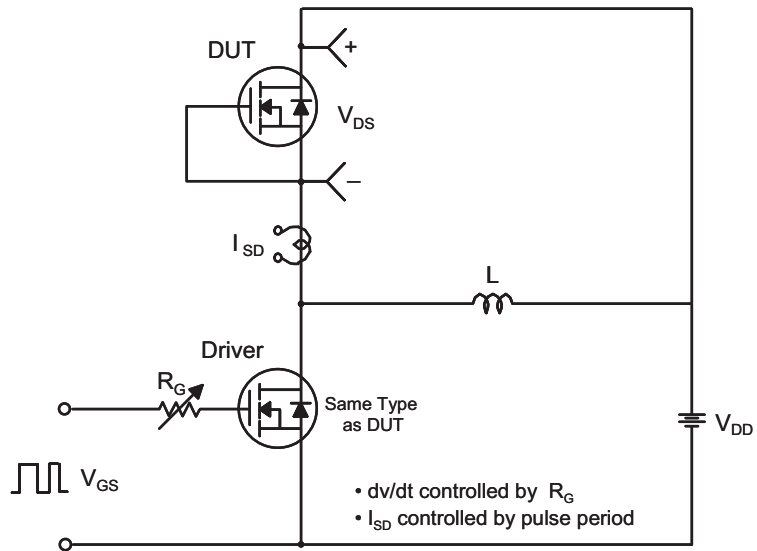
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

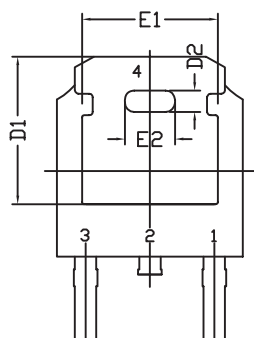
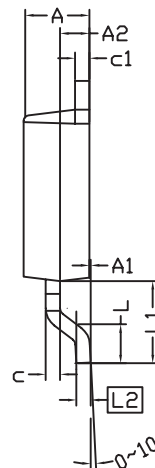
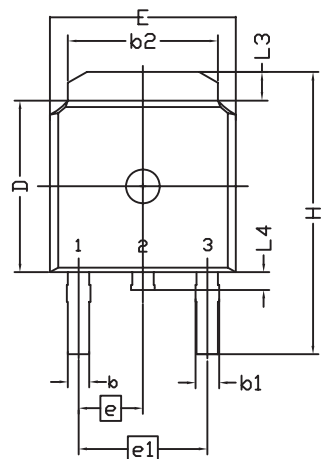


Peak Diode Recovery dv/dt Test Circuit & Waveforms



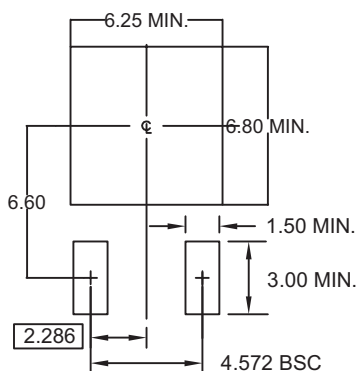
Document No.	PO-00009
Version	S

TO252(DPAK) PACKAGE OUTLINE



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	-----	0.127	0.000	-----	0.005
A2	0.889	1.041	1.143	0.035	0.041	0.045
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.762	0.840	1.143	0.030	0.033	0.045
b2	4.953	5.340	5.461	0.195	0.210	0.215
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.610	0.018	0.020	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
D2	0.662	0.762	0.862	0.026	0.030	0.034
E	6.350	6.604	6.731	0.250	0.260	0.265
E1	4.318	4.826	4.901	0.170	0.190	0.193
E2	1.678	1.778	1.878	0.066	0.070	0.074
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.414	0.370	0.395	0.410
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.635	-----	1.016	0.025	-----	0.040

RECOMMENDED LAND PATTERN



UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)

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