MT21P02N2

P-Channel Enhancement Mode Field Effect Transistor

MT Semiconductor®

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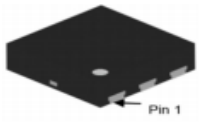
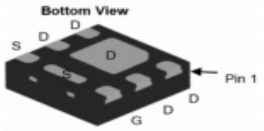
Product Summary

- V_{DS}= -20V
- I_D= -15A
- $R_{DS(ON)}$ =15mΩ@V_{GS}= -4.5V
- $R_{DS(ON)}$ =21mΩ@V_{GS}= -2.5V

DFN2020-6L



Top View



Bottom View

Features

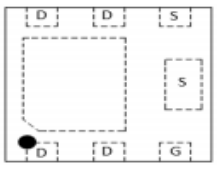
- Low Gate Charge
- Excellent $R_{DS(ON)}$
- Fast Switching Speed

Applications

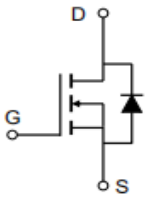
- Load Switch
- PWM Application
- Power Management

Mechanical Data

- Case: DFN2020-6L
- Case Material: "Green" Molding Compound. UL-Flammability Classification Rating 94V-0.



Top View
Pin Configuration



Device Symbol

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-120	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-15	A
Drain Current-Pulsed (Note 1)	I_{DM}	-60	A
Maximum Power Dissipation	P_D	2.6	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
R_{thJA}	Maximum Junction-to-Ambient [1]	t≦10 Sec	20	25	℃/W
		Steady State	45	55	

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±8V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250μA	-0.4	-0.68	-1.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-10A		1 1	1 5	mΩ
		V_{GS}=-2.5V, I_D=-5 A		1 5	21	m Ω
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=- 5A		60		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		-0.59	-1	V
I_S	Maximum Body-Diode Continuous Current				-7	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-6V, f=1MHz		1979		pF
C_{oss}	Output Capacitance			213		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-6V, I_D=- 8A		16		nC
Q_{gs}	Gate Source Charge			4		nC
Q_{gd}	Gate Drain Charge			3.0		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-6V, R_L=0.5Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			35		ns
$t_{D(off)}$	Turn-Off DelayTime			71		ns
t_f	Turn-Off Fall Time			70		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=- 8A, dI/dt=100A/ μs		10		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=- 8A, dI/dt=100A/ μs		3		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

Typical Characteristics (@ T_J = 25°C, unless otherwise specified.)

Figure 1: Output Characteristics

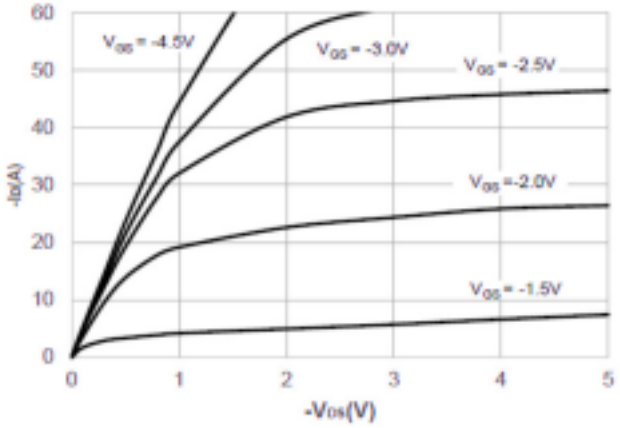


Figure 2: Typical Transfer Characteristics

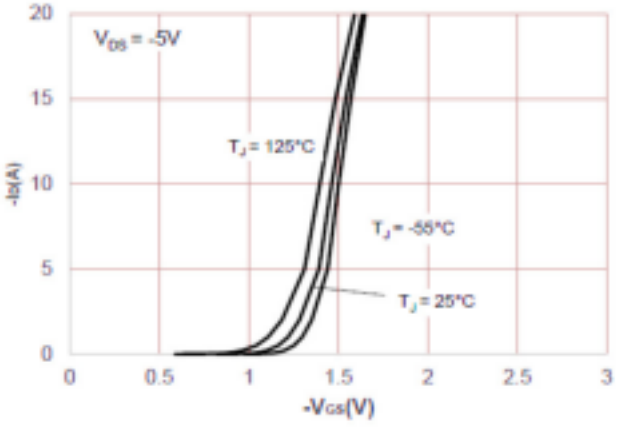


Figure 3: On-resistance vs. Drain Current

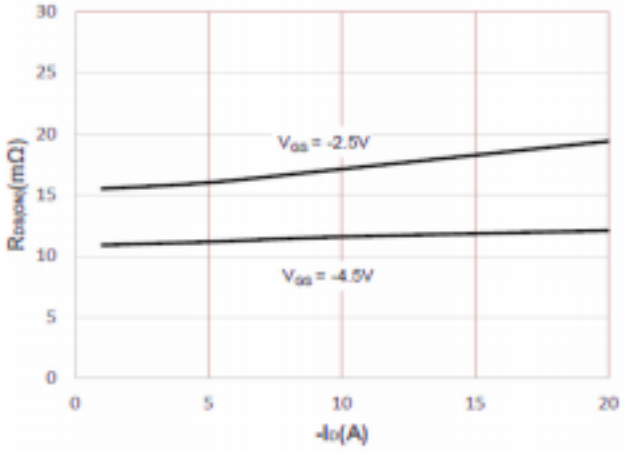


Figure 4: Body Diode Characteristics

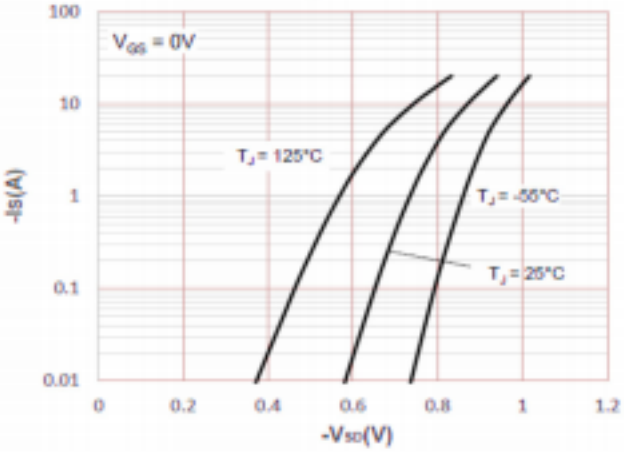


Figure 5: Gate Charge Characteristics

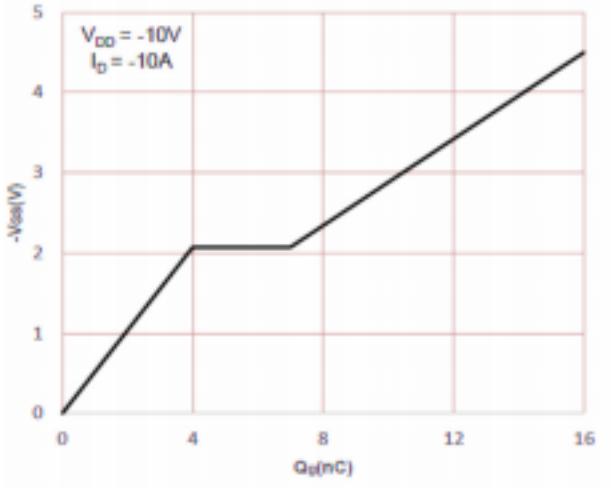
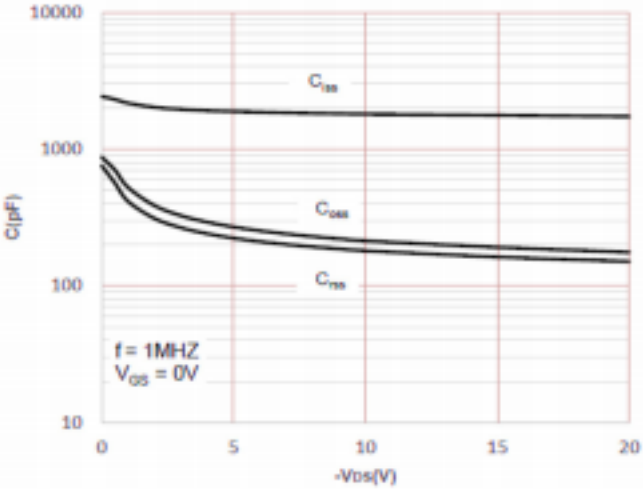


Figure 6: Capacitance Characteristics



Typical Characteristics (@ T_J = 25°C, unless otherwise specified.)

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

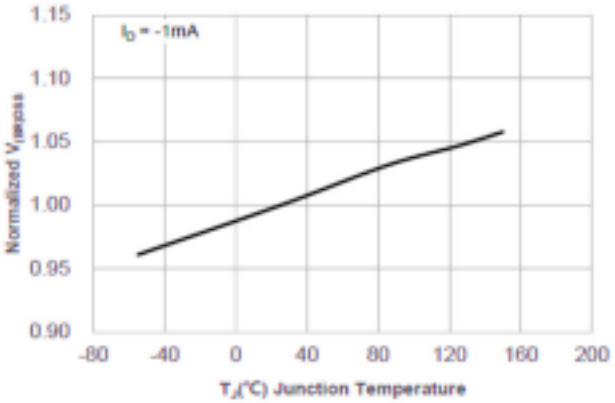


Figure 8: Normalized on Resistance vs. Junction Temperature

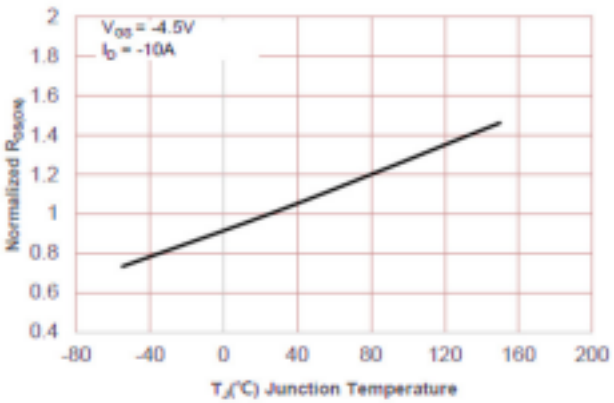


Figure 9: Maximum Safe Operating Area

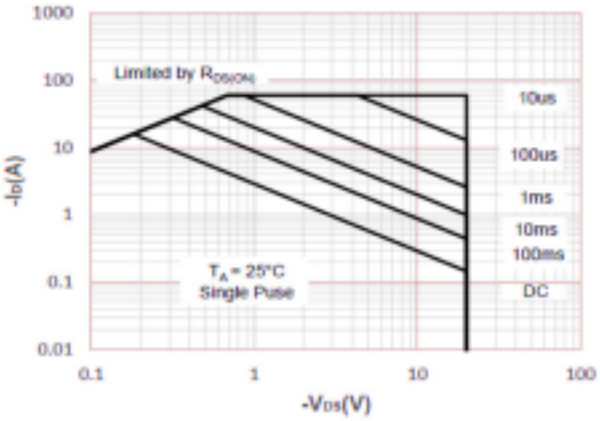


Figure 10: Maximum Continuous Drian Current vs. Ambient Temperature

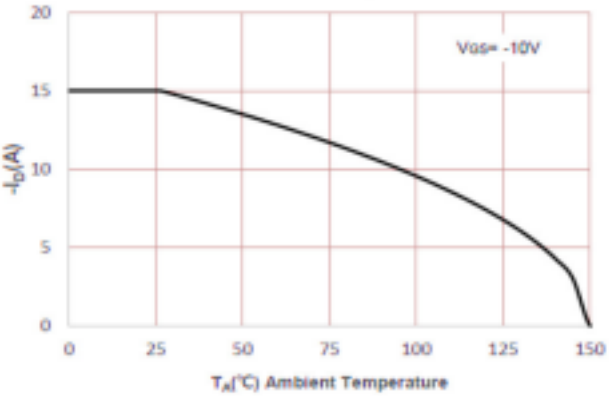


Figure 11: Normalized Maximum Transient Thermal Impedance

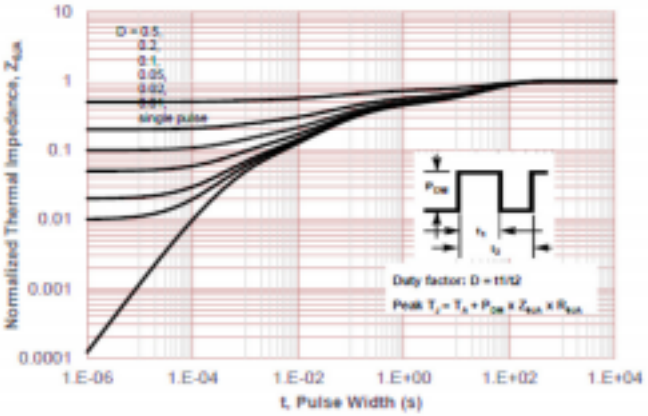
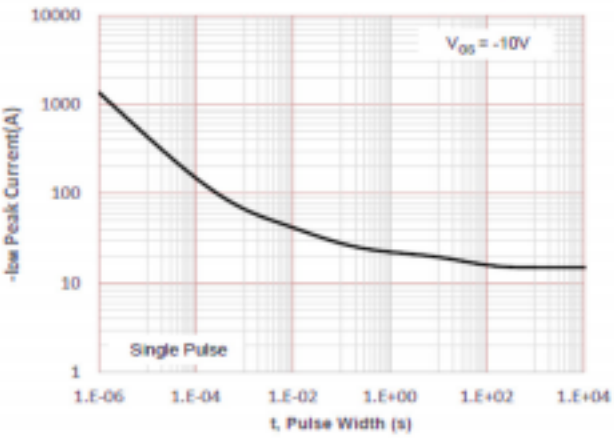
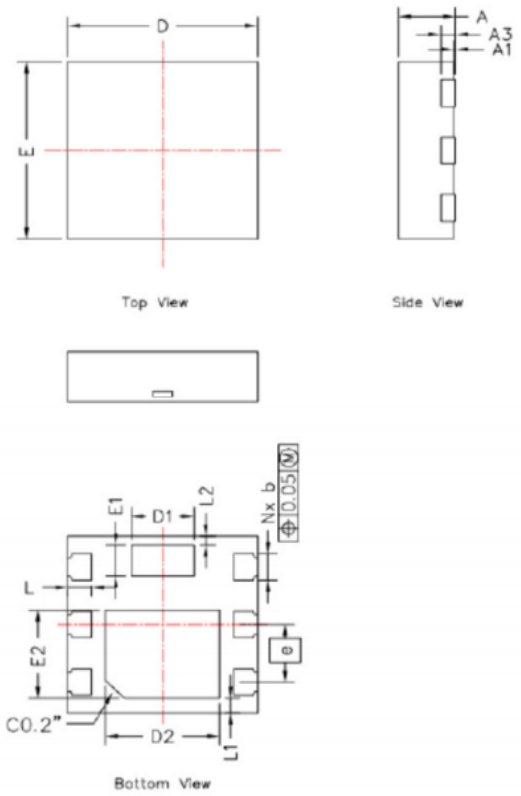


Figure 12: Peak Current Capacity



DFN2020-6L Package Information

Package Outline



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.195	0.203	0.211	0.008	0.008	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65BSC			0.026 BSC		
D	1.900	2.000	2.100	0.075	0.079	0.083
E	1.900	2.000	2.100	0.075	0.079	0.083
D1	0.560	0.660	0.760	0.022	0.026	0.030
E1	0.250	0.350	0.450	0.010	0.014	0.018
D2	1.100	1.200	1.300	0.043	0.047	0.051
E2	0.900	1.000	1.100	0.035	0.039	0.043
L	0.150	0.250	0.350	0.006	0.010	0.014
L1	0.065	0.165	0.265	0.003	0.006	0.010
L2	0.000	0.100	0.200	0.000	0.004	0.008

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