# MT3007N3

# P-Channel Enhancement Mode Field Effect Transistor

# **Product Summary**

- VDS= -30V
- ID= -12A
- RDS(ON)  $\leq$  11m  $\Omega$  @VGS= -10V
- RDS(ON)  $\leq$  13m  $\Omega$  @VGS= -4.5V

### **Features**

- · Advanced Trench Process Technology.
- · High Density Cell Design for Ultra Low
- · On-Resistance.
- · Lead free product is acquired.
- · RoHS Compliant.

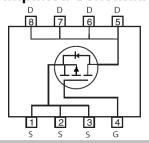
# **Applications**

- · Notebook Computer
- · Portable Battery Pack

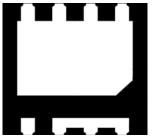
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# **Simplified Schematic**



MARKING DIAGRAM & PIN ASSIGNMENT



DFN3X3-8L

# **Absolute Maximum Ratings** (T<sub>A</sub> = 25 °C unless otherwise noted)

PIN1

Symbol	Parameter	10s	Steady State	Units
VDS	Drain-Source Voltage	-30		V
V <sub>G</sub> S	Gate-Source Voltage	±20		V
I <sub>D</sub>	Continuous Drain Current <sup>1</sup>	-14	-12	Α
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-60		А
Is	Continuous Source Current (Diode Conduction) <sup>1</sup>	-5.2	-4.2	Α
PD	Maximum Power Dissipation <sup>1</sup>	3.0	1.5	W
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction and Storage Temperature Range	-55 to 150		${\mathbb C}$

# **Thermal Resistance Ratings**

Symbol	Parameter		Typical	Maximum	Unit	
R <sub>thJA</sub>	Maximum Junction-to-Ambient <sup>1</sup>	t≦10 Sec	33	42	°C/W	
		Steady State	70	82	C/VV	

### Notes:

- 1. Surface Mounted on 1" x 1" FR4 Board.
- 2. Pulse width limited by maximum junction temperature.

# Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit	
• Stati	c Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-0.8	-1	-1.3	V	
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	-	-	±100	nA	
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	-	-	-1	μА	
I <sub>DSS</sub>		$V_{DS}$ = -24V, $V_{GS}$ = 0V, $T_{J}$ = $85$ $^{\circ}\mathrm{C}$	-	-	-5		
П	Drain Source On State Resistance <sup>a</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	10	11	mΩ	
$R_{DS(on)}$		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A	-	12	13		
g <sub>fs</sub>	Forward Transconductance <sup>a</sup>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -9A	-	40	-	S	
V <sub>SD</sub>	Diode Forward Voltage <sup>a</sup>	I <sub>S</sub> = - 1 A, V <sub>GS</sub> = 0V	-	-	-1.3	V	
• Dyna	imic Characteristics <sup>b</sup>						
Ciss	Input Capacitance		-	3780.0	-		
Coss	Output Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz	-	576.0	-	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	485.0	-		
Qg	Total Gate Charge		-	42	-		
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -5V, I <sub>D</sub> = -13A	-	15	-	nC	
Q <sub>gd</sub>	Gate-Drain Charge		-	11	-		
t <sub>d(on)</sub>	Turn-On Delay Time		-	19.5	-		
t <sub>r</sub>	Rise Time	$V_{DD} = -15V, R_L = 15\Omega$	-	10.0	-	nSec	
$T_{d(off)}$	Turn-Off Delay Time	$I_D = -1A$ , $V_{GEN} = -10V$ , $R_G = 6\Omega$	-	137.5	-		
t <sub>f</sub>	Fall Time		-	55.3	-		
Rg	Gate Resistance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0, f = 1MHz	-	3.4	-	Ω	
t <sub>rr</sub>	Source-Drain Reverse Recovery Time	I <sub>F</sub> = -2.1A, di/dt = 100A/μs	-	60	100	nSec	

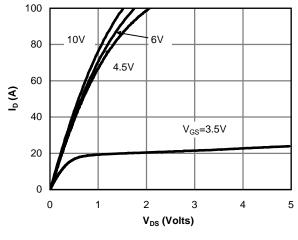
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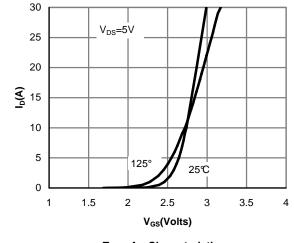
## Note:

a. Pulse test; pulse width≦300µs, duty cycle≦2%.

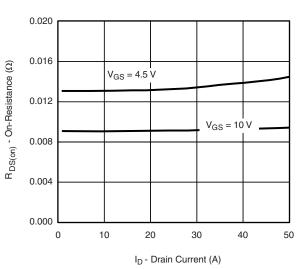
b. Guaranteed by design, not subject to production testing.

# Characteristics Curve (TA=25°C, unless otherwise noted)

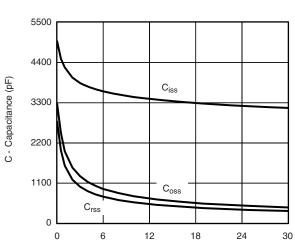




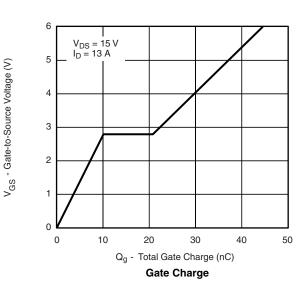




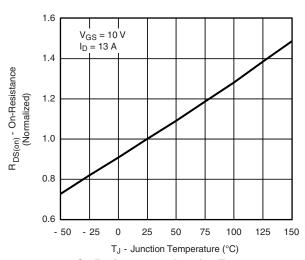
Transfer Characteristics



On-Resistance vs. Drain Current

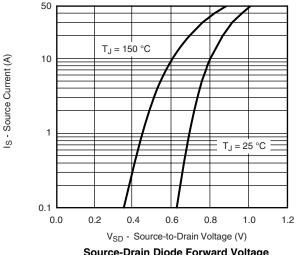


V<sub>DS</sub> - Drain-to-Source Voltage (V) **Capacitance** 

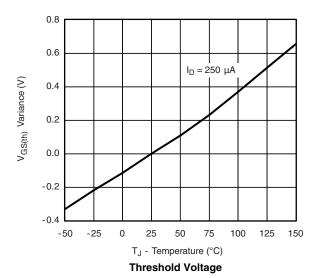


On-Resistance vs. Junction Temperature

# Characteristics Curve (TA=25°C, unless otherwise noted)

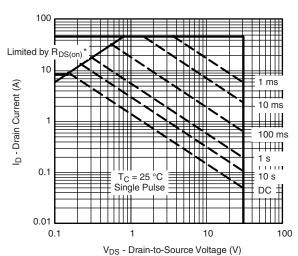


Source-Drain Diode Forward Voltage



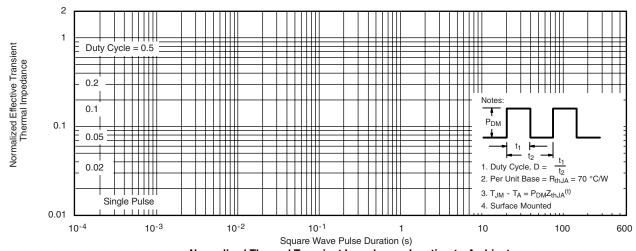
0.030 0.024  $R_{DS(on)}$  - On-Resistance ( $\Omega$ )  $I_D = 13 A$ 0.018 0.012 0.006 0.000 0 10  $V_{\text{GS}}$  - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



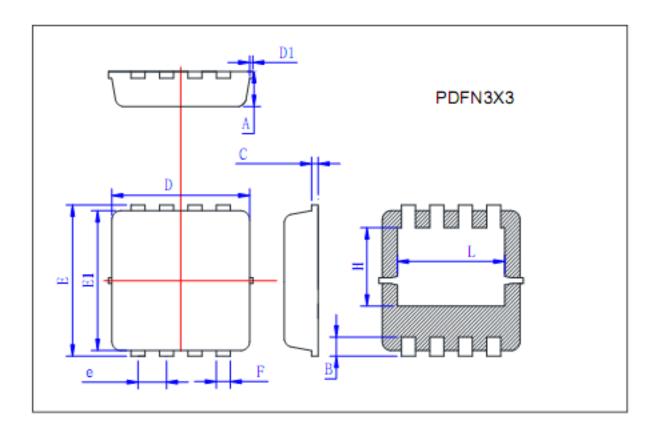
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

# **PACKAGE OUTLINE DIMENSIONS**



Symbol	Min	Тур	Max
A	0.725	0.775	0.825
В	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
El	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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