MT3213

N-Channel Low Qg^{\otimes} MOSFET 30V, 80A, 4.8m Ω

Features

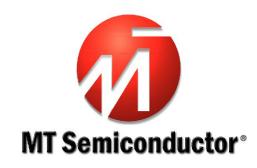
- $R_{DS(ON)} = 4.8 m\Omega$, $V_{GS} = 10 V$, $I_{D} = 40 A$
- High performance trench technology for extremely low RDS(ON)
- · Low gate charge
- · High power and current handling capability

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conven tional swit ching PWM controllers. It has been optimized for low gate charge, low $r_{\mbox{\footnotesize{DS}}(\mbox{\footnotesize{ON}})}$ and fast switching speed.

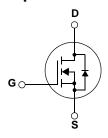
Applications

- · DC-DC primary bridge
- · DC-DC Synchronous rectification
- Hot swap

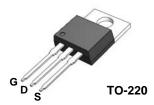


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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current	00	
	Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 10V$) (Note 1)	80	Α
	Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 4.5V$) (Note 1)	65	Α
	Continuous ($T_{amb} = 25^{\circ}C$, $V_{GS} = 10V$, with $R_{\theta JA} = 62^{\circ}C/W$)	15	А
	Pulsed	Figure 4	Α
E _{AS}	Single Pulse Avalanche Energy (Note 2)	190	mJ
P_{D}	Power dissipation	36	W
	Derate above 25°C	0.73	W/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	3	°C/W
$R_{\theta,JA}$	Thermal Resistance Junction to Ambient TO-220 (Note 3)	62.5	°C/W

Package Marking and Ordering Information

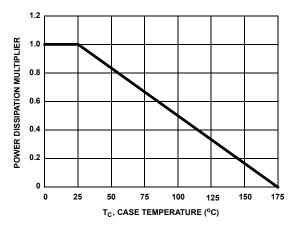
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT3213	MT3213	TO-220AB	Tube	N/A	50 units

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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30	-	-	V
		V _{DS} = 24V	-	-	1	μΑ
I _{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_C = 150^{\circ}C$	-	-	250	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20V	-	-	±100	nA
On Chara	cteristics					
V _{GS(TH)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.3	1.8	2.5	V
		1 = 400 \/ = 40\/		0.0040		
r	Drain to Source On Resistance	$I_D = 40A, V_{GS} = 10V$	-	0.0048	-	Ω
r _{DS(ON)}	Diam to oddice on resistance	$I_D = 40A$, $V_{GS} = 10V$,	_	0.0082	0.0090	32
		$T_{J} = 175^{\circ}C$		0.0002	0.0000	1
Dynamic	Characteristics					
C _{ISS}	Input Capacitance		-	2139	-	pF
C _{OSS}	Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1MHz	-	464	-	pF
C _{RSS}	Reverse Transfer Capacitance	I = IMHZ	-	199	-	pF
R _G	Gate Resistance	V _{GS} = 0.5V, f = 1MHz	-	1.9	-	Ω
Q _{g(TOT)}	Total Gate Charge at 10V	V _{GS} = 0V to 10V	-	56	72	nC
Q _{q(5)}	Total Gate Charge at 5V	V _{GS} = 0V to 5V	-	30	38	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 1V$ $V_{DD} = 15V$	-	3.0	4.0	nC
Q _{gs}	Gate to Source Gate Charge	$I_D = 40A$ $I_Q = 1.0 \text{mA}$	-	9.0	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	6.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	11	-	nC
Switching	Characteristics (V _{GS} = 10V)					
t _{ON}	Turn-On Time		-	-	207	ns
t _{d(ON)}	Turn-On Delay Time		-	10	-	ns
t _r	Rise Time	V _{DD} = 15V, I _D = 40A	-	128	-	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = 4.5V, R_{GS} = 4.7\Omega$	-	44	-	ns
t _f	Fall Time		-	31	-	ns
t _{OFF}	Turn-Off Time		-	-	112	ns
Drain-Sou	urce Diode Characteristics					
		I _{SD} = 40A	-	-	1.25	V
V_{SD}	Source to Drain Diode Voltage	I _{SD} = 20A	-	-	1.0	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 40A$, $dI_{SD}/dt = 100A/\mu s$	-	-	32	ns
Q _{RR}	Reverse Recovered Charge	I _{SD} = 40A, dI _{SD} /dt = 100A/μs	_	-	18	nC

- Package current limitation is 80A.
 Starting T_J = 25°C, L = 51uH, I_{AS} = 64A, V_{DD} = 27V, V_{GS} = 10V.
 Pulse width = 100s.





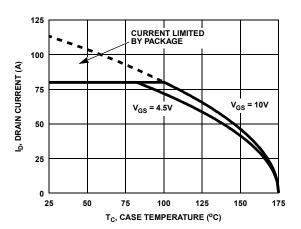


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

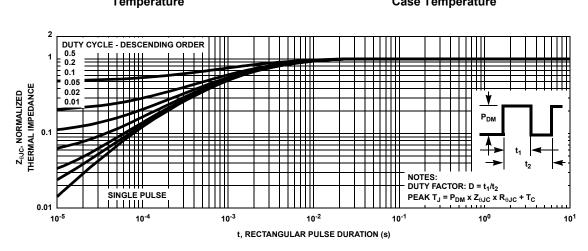


Figure 3. Normalized Maximum Transient Thermal Impedance

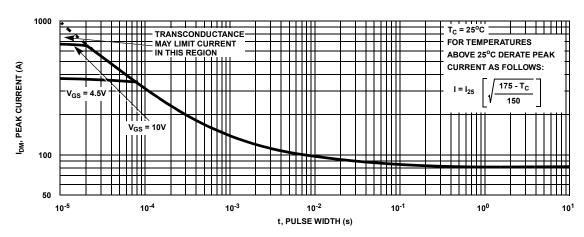


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted 1000 500 If R = 0 $t_{AV} = (L)(I_{AS})/(1.3*RATED BV_{DSS} - V_{DD})$ IAS, AVALANCHE CURRENT (A) $t_{AV} = (L/R)ln[(l_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD})]$ 100 100 DRAIN CURRENT (A) STARTING $T_J = 25^{\circ}C$ 10 OPERATION IN THIS AREA MAY BE LIMITED BY r_{DS(ON)} SINGLE PULSE T_J = MAX RATED T_C = 25°C 0.1 $$10$ $V_{\rm DS},$ drain to source voltage (V) 0.01 t_{AV}, TIME IN AVALANCHE (ms) NOTE: Refer to Fairchild Application Notes AN7514 and AN7515 Figure 6. Unclamped Inductive Switching Figure 5. Forward Bias Safe Operating Area Capability 160 160 PULSE DURATION = 80µs V_{GS} = 5V DUTY CYCLE = 0.5% MAX V_{GS} = 4V $V_{DD} = 15V$), DRAIN CURRENT (A) 120 DRAIN CURRENT (A) V_{GS} = 10V 80 $V_{GS} = 3V$ ف T_C = 25°C PULSE DURATION = 80µs DUTY CYCLE = 0.5% MAX 0.4 2.0 4.0 V_{GS}, GATE TO SOURCE VOLTAGE (V) V_{DS}, DRAIN TO SOURCE VOLTAGE (V) Figure 7. Transfer Characteristics Figure 8. Saturation Characteristics PULSE DURATION = 80µs DUTY CYCLE = 0.5% MAX PULSE DURATION = 80μs I_D = 40A DUTY CYCLE = 0.5% MAX NORMALIZED DRAIN TO SOURCE ON RESISTANCE 1.6 10 FDS(ON), DRAIN TO SOURCE ON RESISTANCE (mΩ) I_D = 1A 0.8 V_{GS} = 10V, I_D = 40A 2 0.6 -40 0 40 80 120 200 -80 160 V_{GS}, GATE TO SOURCE VOLTAGE (V) T_J, JUNCTION TEMPERATURE (°C) Figure 9. Drain to Source On Resistance vs Gate Figure 10. Normalized Drain to Source On

Voltage and Drain Current

Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

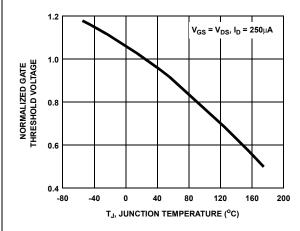


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

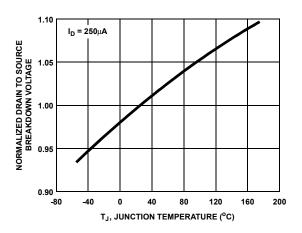


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

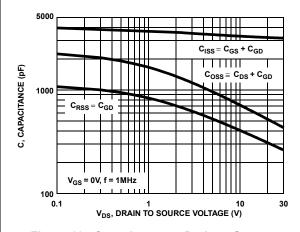


Figure 13. Capacitance vs Drain to Source Voltage

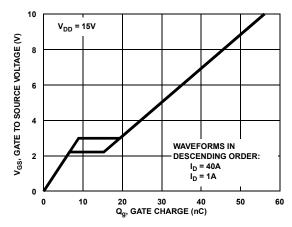


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

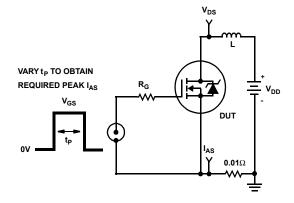


Figure 15. Unclamped Energy Test Circuit

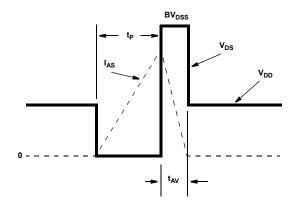


Figure 16. Unclamped Energy Waveforms

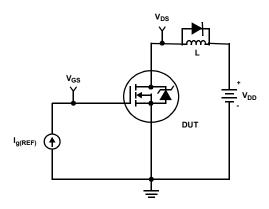


Figure 17. Gate Charge Test Circuit

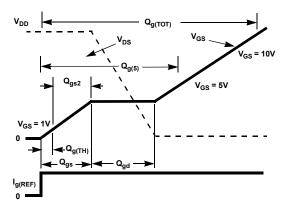


Figure 18. Gate Charge Waveforms

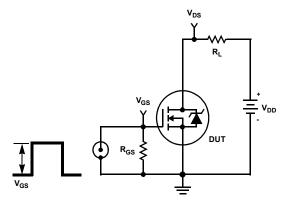


Figure 19. Switching Time Test Circuit

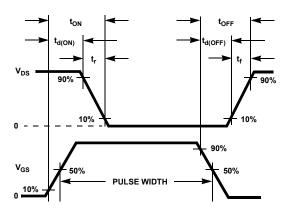


Figure 20. Switching Time Waveforms

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