

MT3240B/B

N-Channel Low Qg[®] MOSFET
40V, 208A, 2.5mΩ

Features

- Max R_{DS(on)}=2.5mΩ at V_{GS}=10V, I_D=40A
- High performance trench technology for extremely low R_{DS(on)}
- Low Gate Charge
- High power and current handing capability

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low R_{DS(ON)} and fast switching speed.

Applications

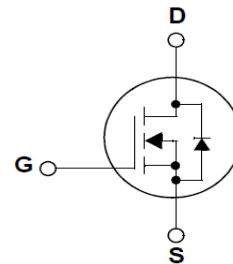
- DC-DC primary bridge
- DC-DC Synchronous rectification
- Power Management for Inverter Systems



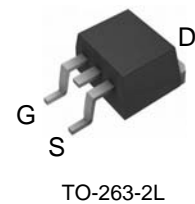
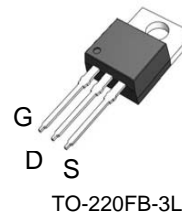
MT Semiconductor[®]

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



		<p>Package Code</p> <p>MT3240B: T0-220FB-3L MT3240BB: T0-263-2L</p>
		<p>Date Code</p> <p>PYWWM</p>
		<p>Lot No</p> <p>XX</p>

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain to Source Voltage	40	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current	208	A
	Continuous (T _C = 25°C, V _{GS} = 10V) (Note 1)		
	Continuous (T _C = 25°C, V _{GS} = 4.5V) (Note 1)	108	A
	Continuous (T _{amb} = 25°C, V _{GS} = 10V, with R _{θJA} = 62°C/W)	35	A
	Pulsed	Figure 4	A
E _{AS}	Single Pulse Avalanche Energy (Note 2)	1.4	J
P _D	Power dissipation	217	W
	Derate above 25°C	0.69	W/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	0.69	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220 (Note 3)	62.5	$^{\circ}\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT3240B	MT3240B	TO-220FB-3L	Tube	N/A	50 units
MT3240BB	MT3240BB	TO-263-2L	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^{\circ}\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	-	3.0	-	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 40\text{A}$, $V_{GS} = 10\text{V}$	-	2.5	-	m Ω
		$I_D = 40\text{A}$, $V_{GS} = 4.5\text{V}$	-	-	-	
		$I_D = 40\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^{\circ}\text{C}$	-	-	-	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	5712	-	pF
C_{OSS}	Output Capacitance		-	1465	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	596	-	pF
R_G	Gate Resistance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$, $f = 1\text{MHz}$	-	1	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	158	-	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	-	30	38	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V	-	3.0	4.0	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 40\text{A}$ $I_g = 1.0\text{mA}$	-	30	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	6.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	66	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}$, $I_D = 40\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 4.7\Omega$	-	35	-	ns
$t_{d(ON)}$	Turn-On Delay Time		-	20	-	ns
t_r	Rise Time		-	20	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	44	-	ns
t_f	Fall Time		-	45	-	ns
t_{OFF}	Turn-Off Time		-	62	-	ns

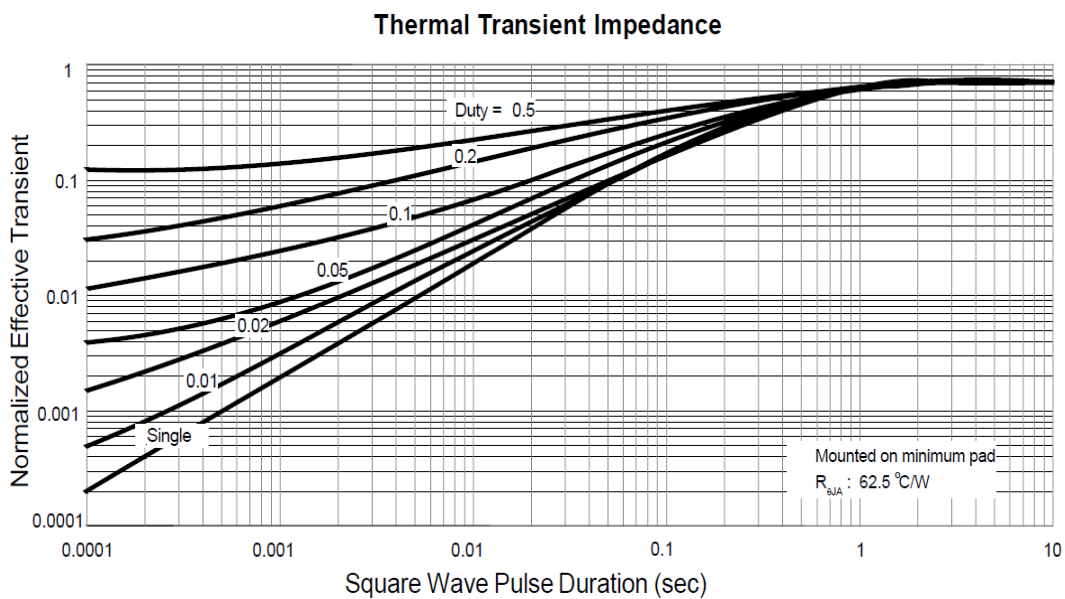
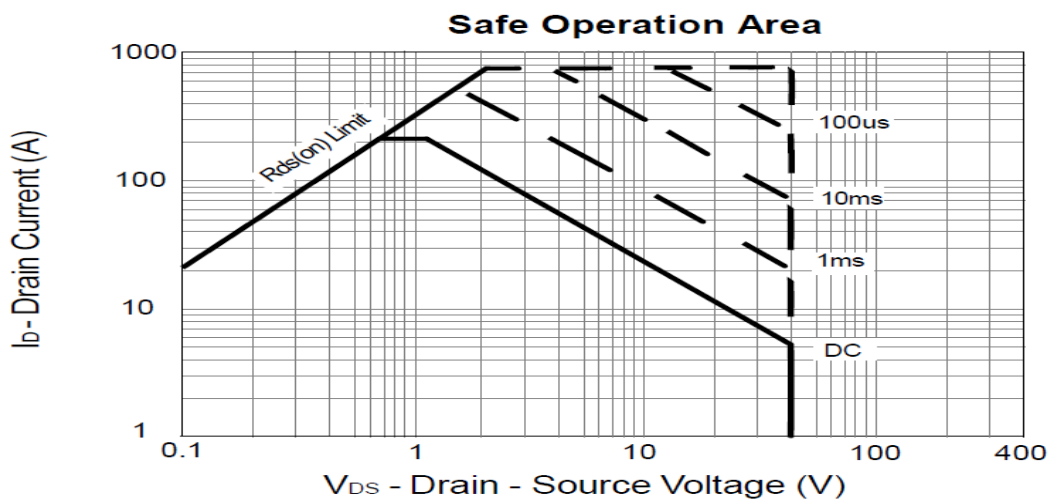
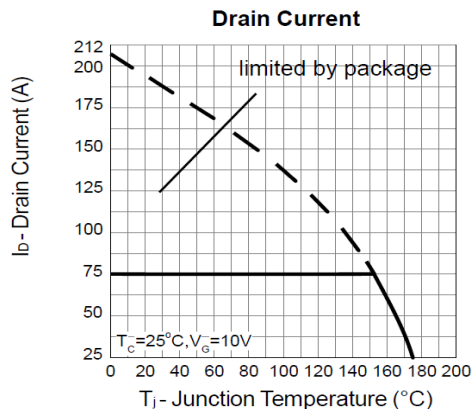
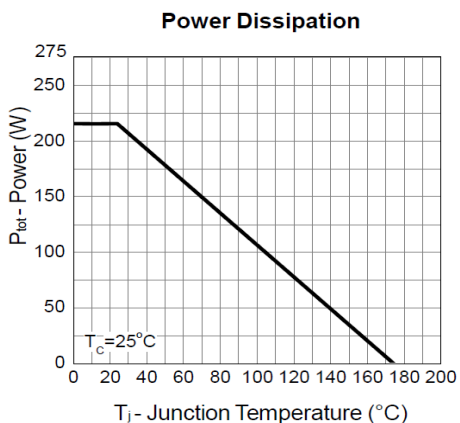
Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 40\text{A}$	-	-	1.25	V
		$I_{SD} = 20\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 40\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	32	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 40\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	18	nC

Notes:

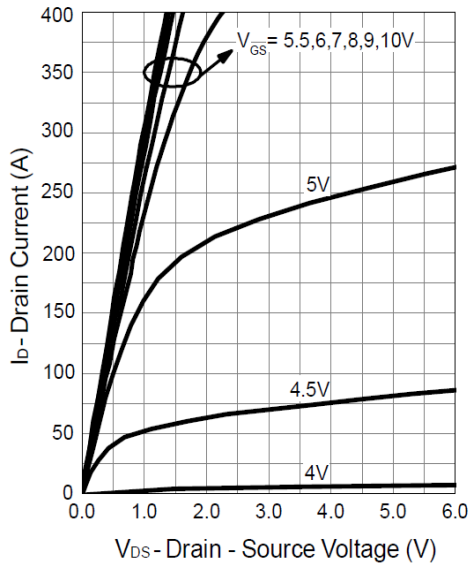
- 1: Package current limitation is 80A.
- 2: Starting $T_J = 25^{\circ}\text{C}$, $L = 0.3\text{mH}$ $I_{AS} = 64\text{A}$, $V_{DD} = 37\text{V}$, $V_{GS} = 10\text{V}$.
- 3: Pulse width = 100s.

Typical Operating Characteristics

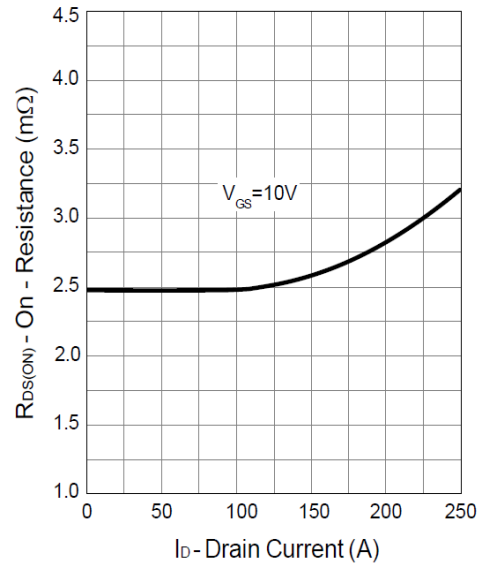


Typical Operating Characteristics (Cont.)

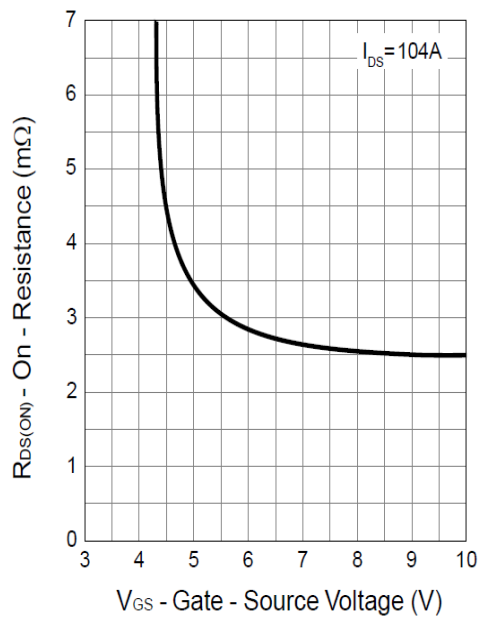
Output Characteristics



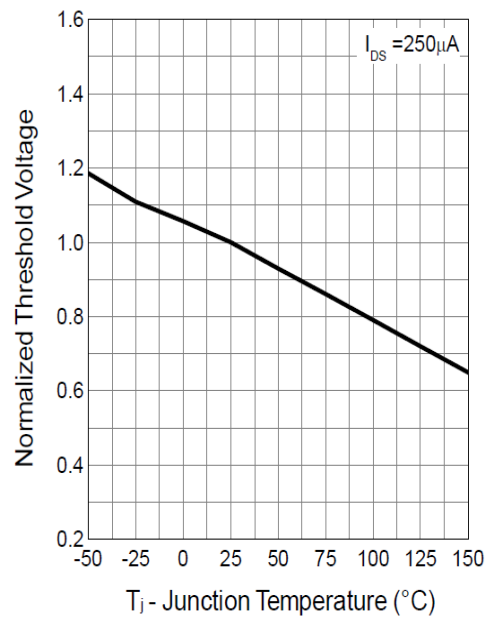
Drain-Source On Resistance



Gate-Source On Resistance

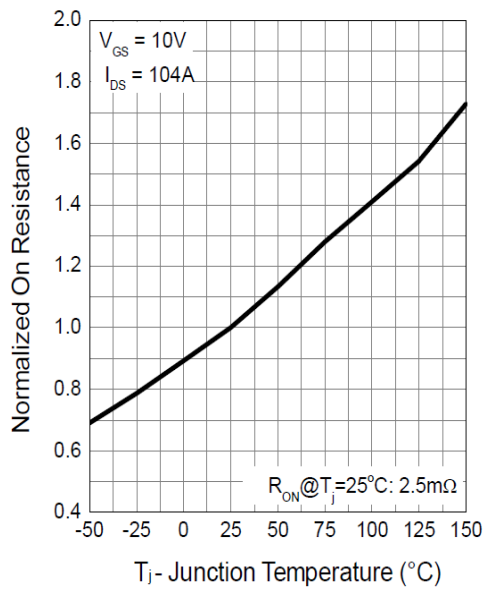


Gate Threshold Voltage

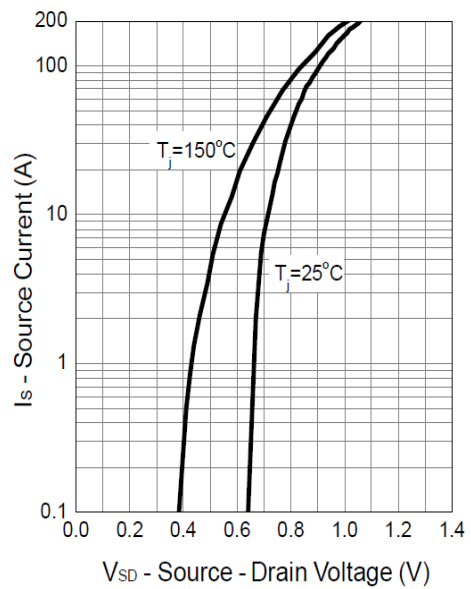


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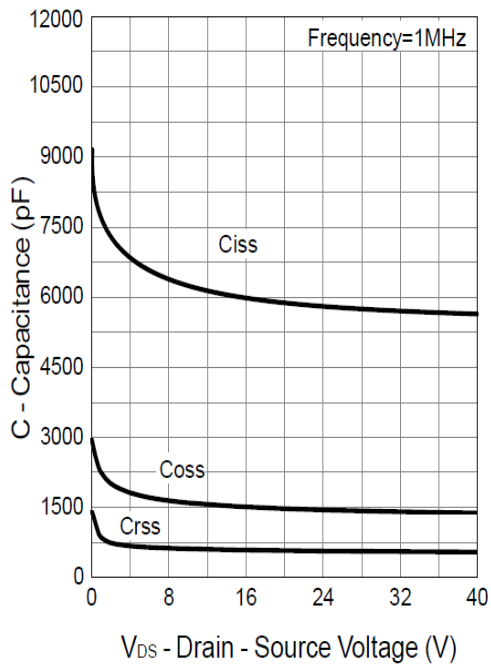
Drain-Source On Resistance



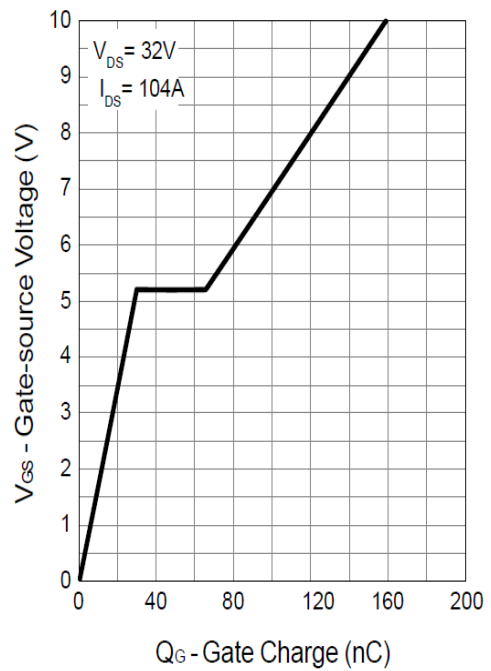
Source-Drain Diode Forward



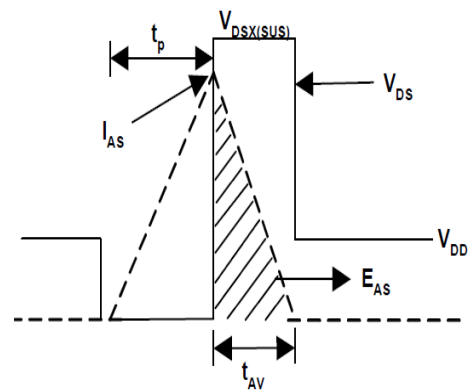
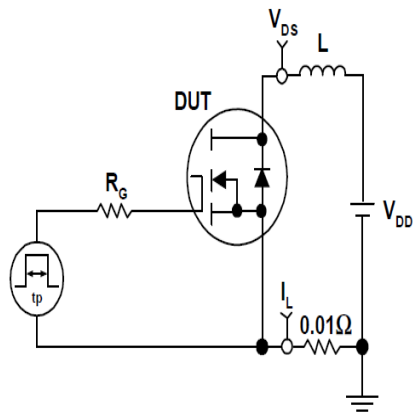
Capacitance



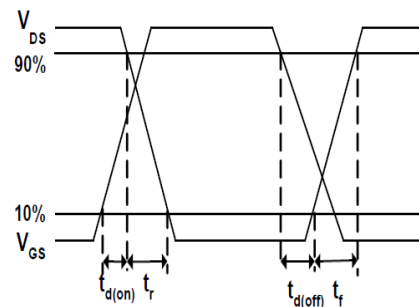
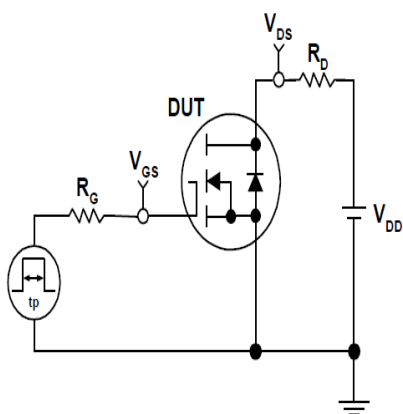
Gate Charge



Avalanche Test Circuit and Waveforms

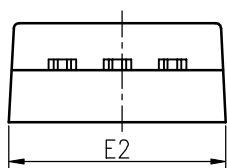
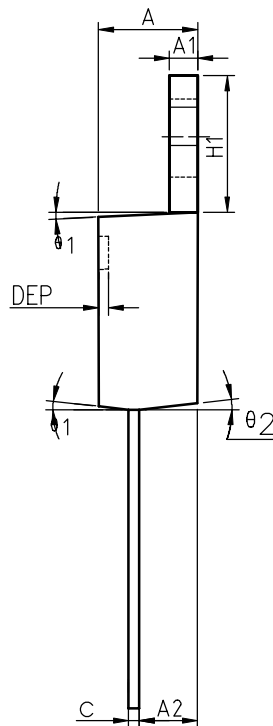
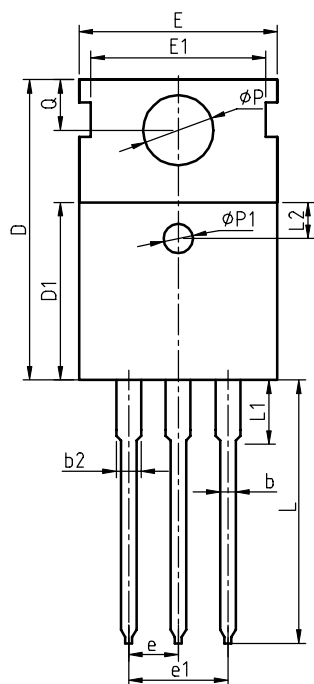


Avalanche Test Circuit and Waveforms



Package Information

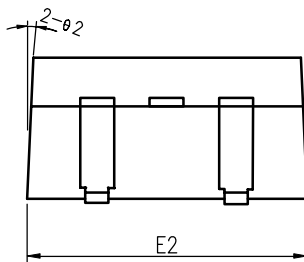
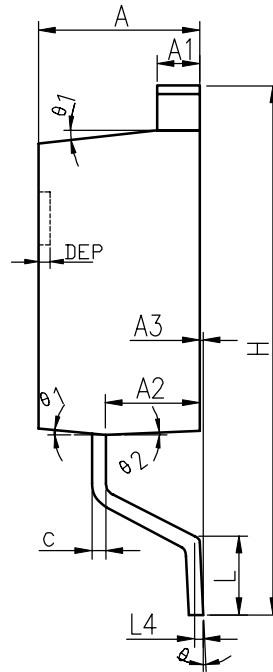
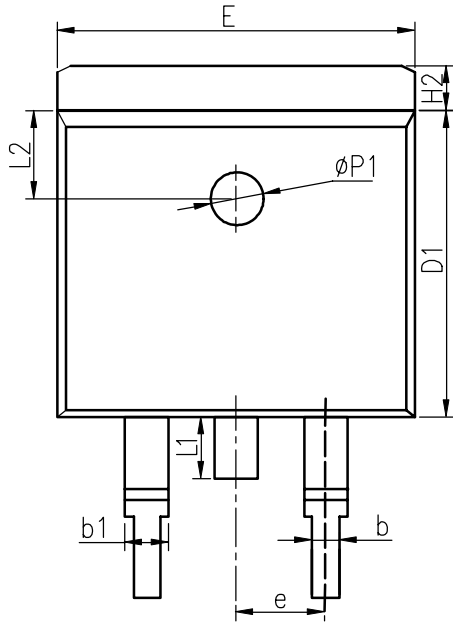
TO-220FB-3L



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
$\theta 1$	5°	7°	9°	5°	7°	9°
$\theta 2$	1°	3°	5°	1°	3°	5°
$\theta 3$	1°	3°	5°	1°	3°	5°

TO-263-2L



COMMON DIMENSIONS

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.22	1.27	1.32	0.048	0.050	0.052
A2	2.59	2.69	2.79	0.102	0.106	0.110
A3	0.00	0.10	0.20	0.000	0.004	0.008
b	0.77	0.813	0.90	0.030	0.032	0.035
b1	1.20	1.270	1.36	0.047	0.050	0.054
c	0.34	0.381	0.47	0.013	0.015	0.019
D1	8.60	8.70	8.80	0.339	0.343	0.346
E	10.00	10.16	10.26	0.394	0.400	0.404
E2	10.00	10.10	10.20	0.394	0.398	0.402
e	2.54 BSC			0.100 BSC		
H	14.70	15.10	15.50	0.579	0.594	0.610
H2	1.17	1.27	1.40	0.046	0.050	0.055
L	2.00	2.30	2.60	0.079	0.091	0.102
L1	1.45	1.55	1.70	0.057	0.061	0.067
L2	2.50 REF			0.098 REF		
L4	0.25 BSC			0.010 BSC		
	0°	5°	8°	0°	5°	8°
1	5°	7°	9°	5°	7°	9°
2	1°	3°	5°	1°	3°	5°
$\phi P1$	1.40	1.50	1.60	0.055	0.059	0.063
DEP	0.05	0.10	0.20	0.002	0.004	0.008

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10. 本公司一直致力于提高产品的质量和可靠性, 但一般来说, 半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失, 希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等, 这是作为机器和系统的出厂保证。特别是单片机的软件, 由于单独进行验证很困难, 所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
11. 如果把本资料所记载的产品从其载体设备上卸下, 有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时, 请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时, 本公司将不承担任何责任。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.