MT34P50N3

P-Channel Low Qg MOSFET
- 40V,-40A,20mΩ

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Features

- R_{DS} (on)=20mΩ at V_{GS} = -10V,ID= -10A
- High performance trench technology for extremely low R_{DS}(on)
- Low Gate Charge
- High power and current handing capability

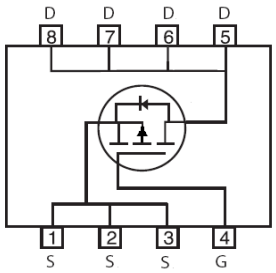
General Description

This P-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

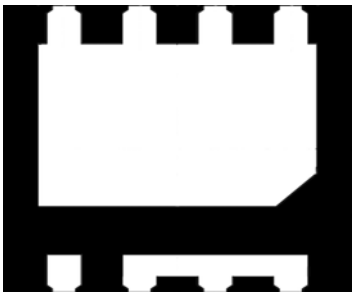
Applications

- DC-DC primary bridge
- DC-DC Synchronous rectification
- Power Managemement for Inverter Systems

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



PIN1

DFN3X3-8L

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-40	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-20	A
Pulsed Drain Current	I_{DM}	-140	A
Maximum Power Dissipation	P_D	60	W
Single pulse avalanche energy (Note 5)	E_{AS}	198	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.88	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

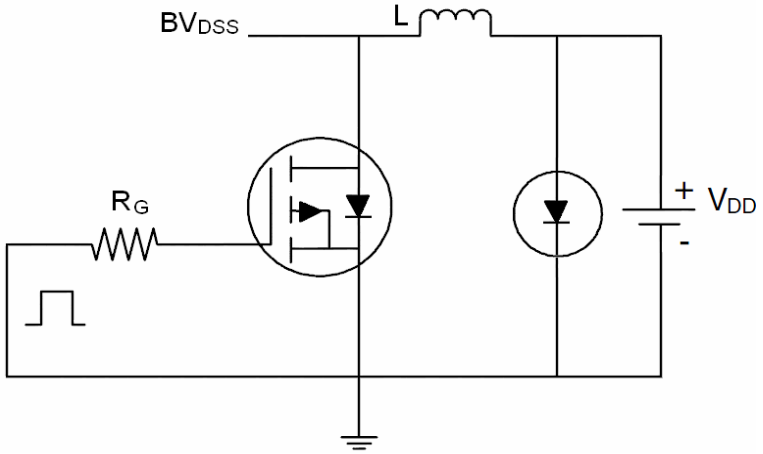
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.9	-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-12A	-	20	26	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-12A	321	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{Iss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	2660	-	PF
Output Capacitance	C_{oss}		-	350	-	PF
Reverse Transfer Capacitance	C_{rss}		-	198	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V,I_D=-20A V_{GS}=-10V,R_G=3Ω	-	10	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	t_f		-	24	-	nS
Total Gate Charge	Q_g	V_{DS}=-20,I_D=-12A, V_{GS}=-10V	-	68		nC
Gate-Source Charge	Q_{gs}		-	13		nC
Gate-Drain Charge	Q_{gd}		-	14		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-20A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-40	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =- 20A di/dt = -100A/μs(Note3)	-	40		nS
Reverse Recovery Charge	Qrr		-	42		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

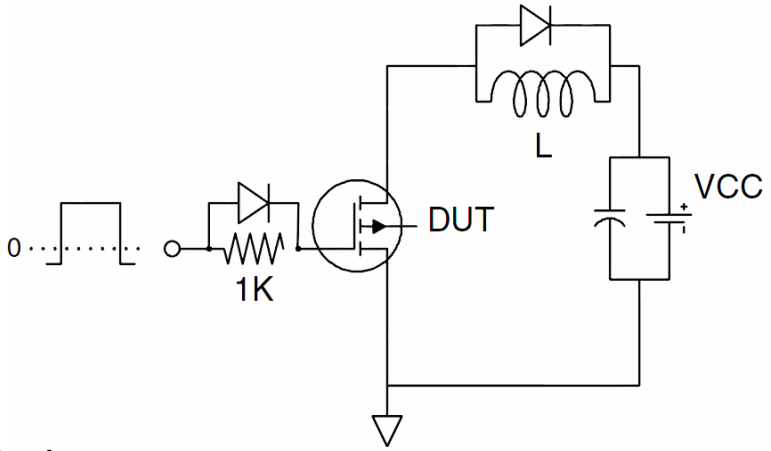
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-20V,V_G=-10V,L=1mH,Rg=25Ω,I_{AS}=33A

Test Circuit

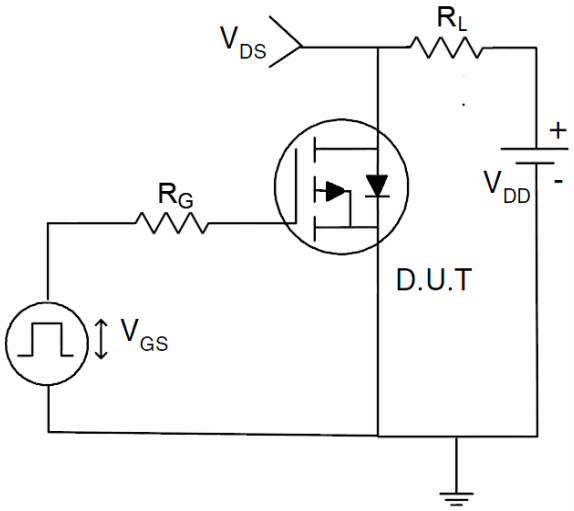
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

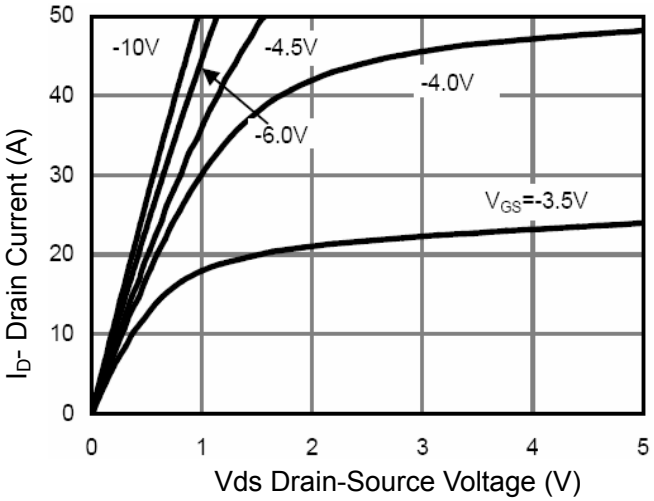


Figure 1 Output Characteristics

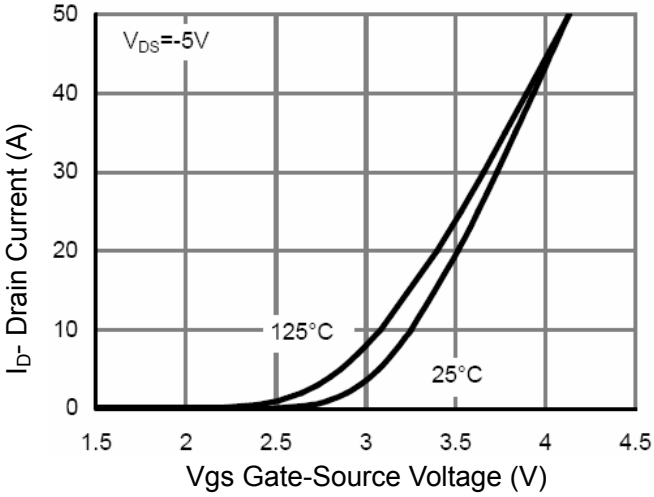


Figure 2 Transfer Characteristics

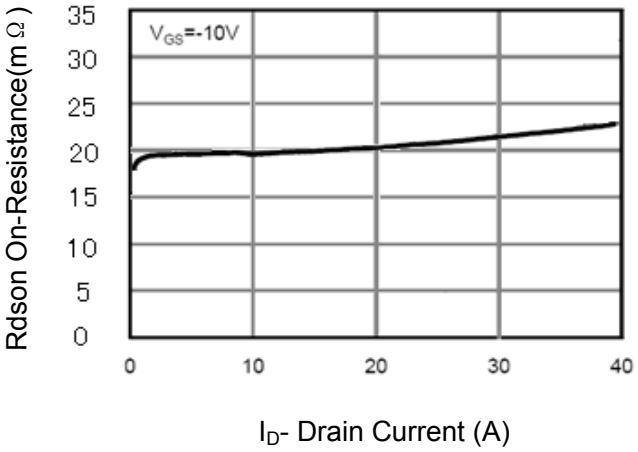


Figure 3 Rdson- Drain Current

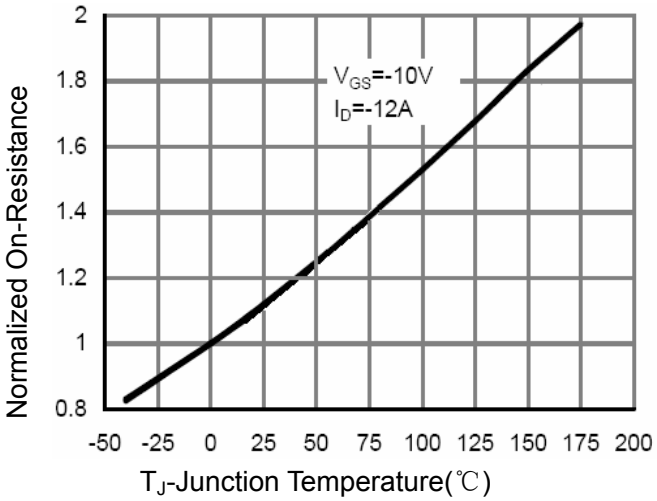


Figure 4 Rdson-Junction Temperature

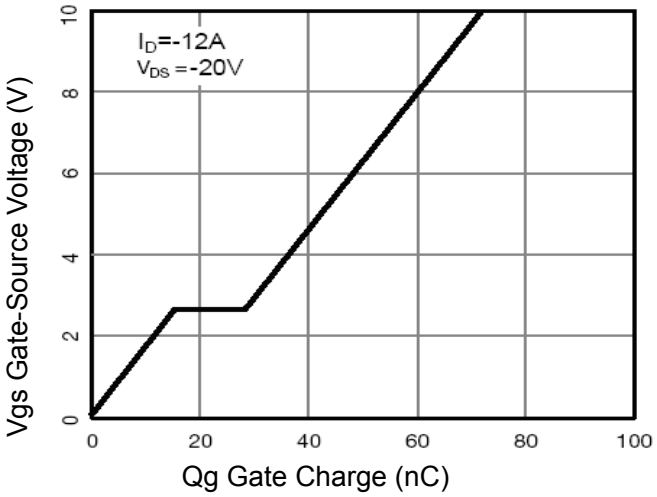


Figure 5 Gate Charge

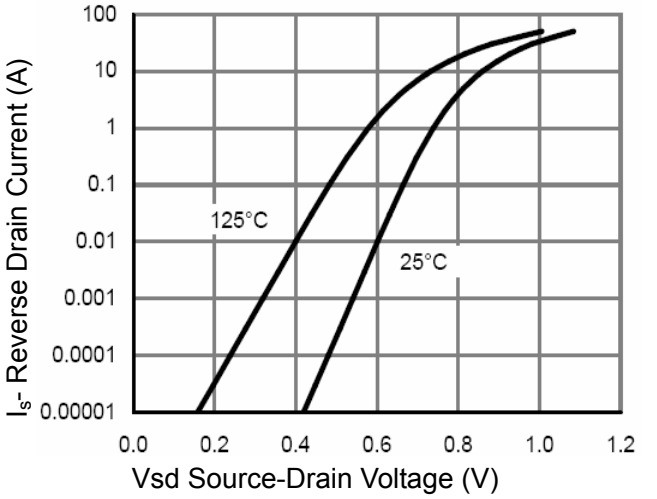


Figure 6 Source- Drain Diode Forward

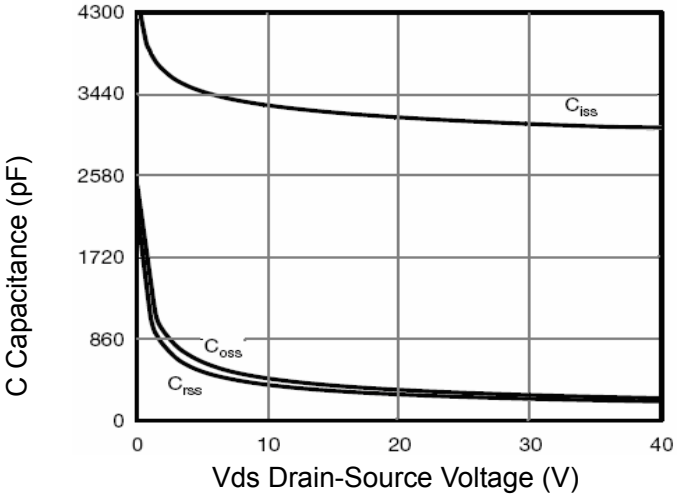


Figure 7 Capacitance vs Vds

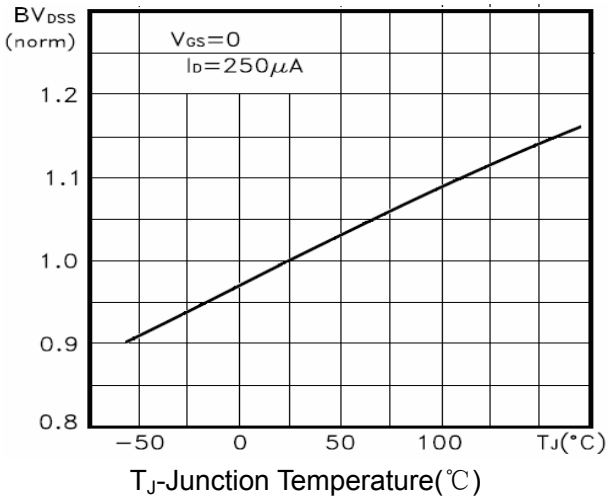


Figure 9 BV_{DSS} vs Junction Temperature

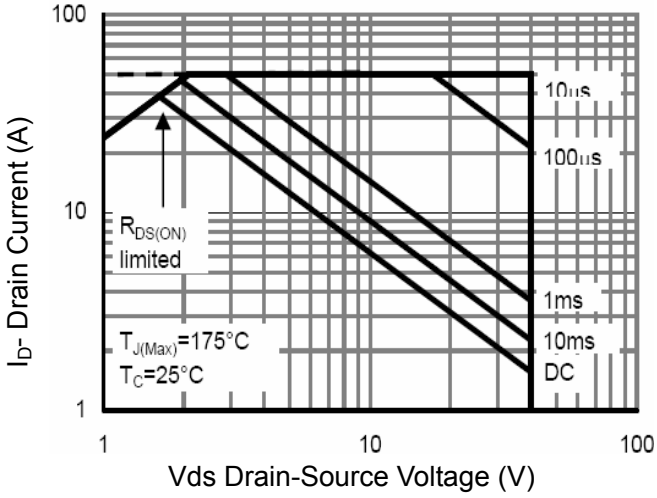


Figure 8 Safe Operation Area

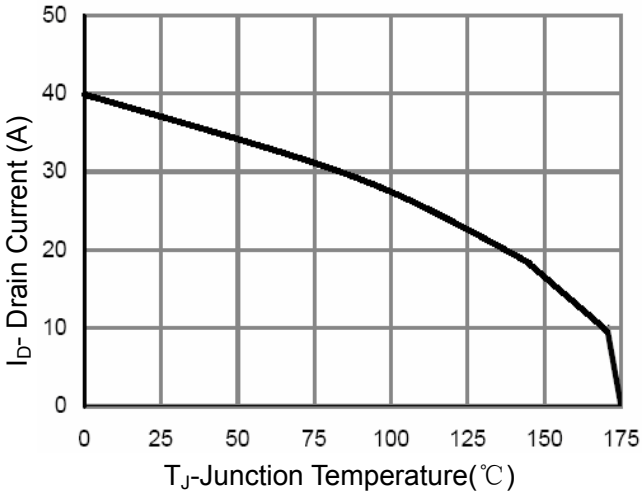


Figure 10 ID Current Derating vs Junction Temperature

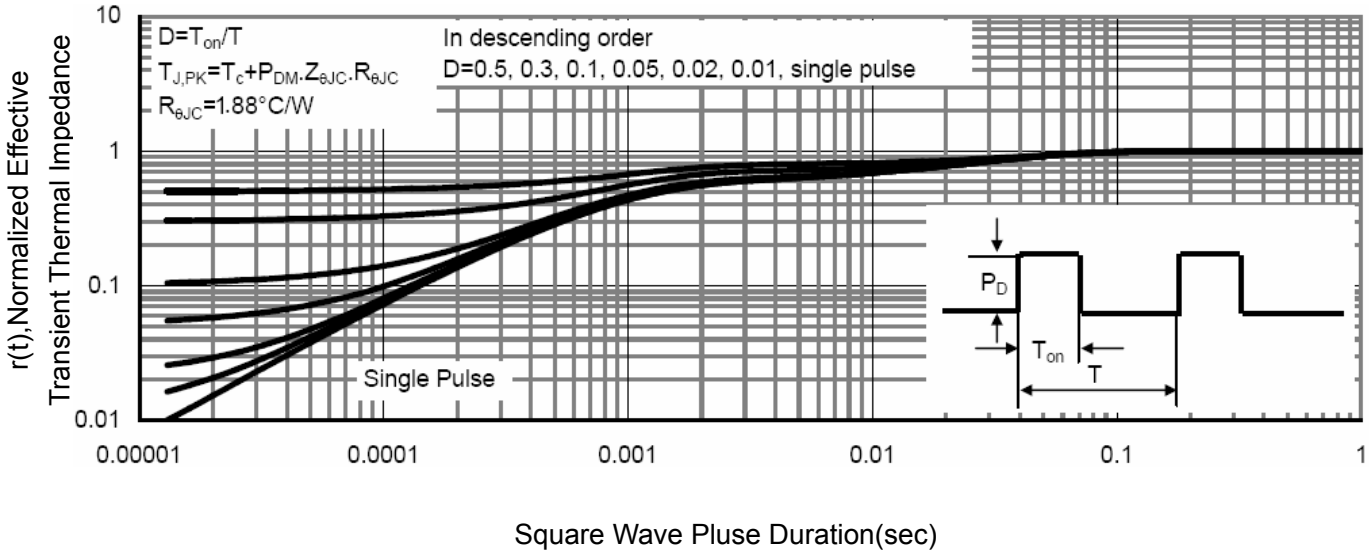
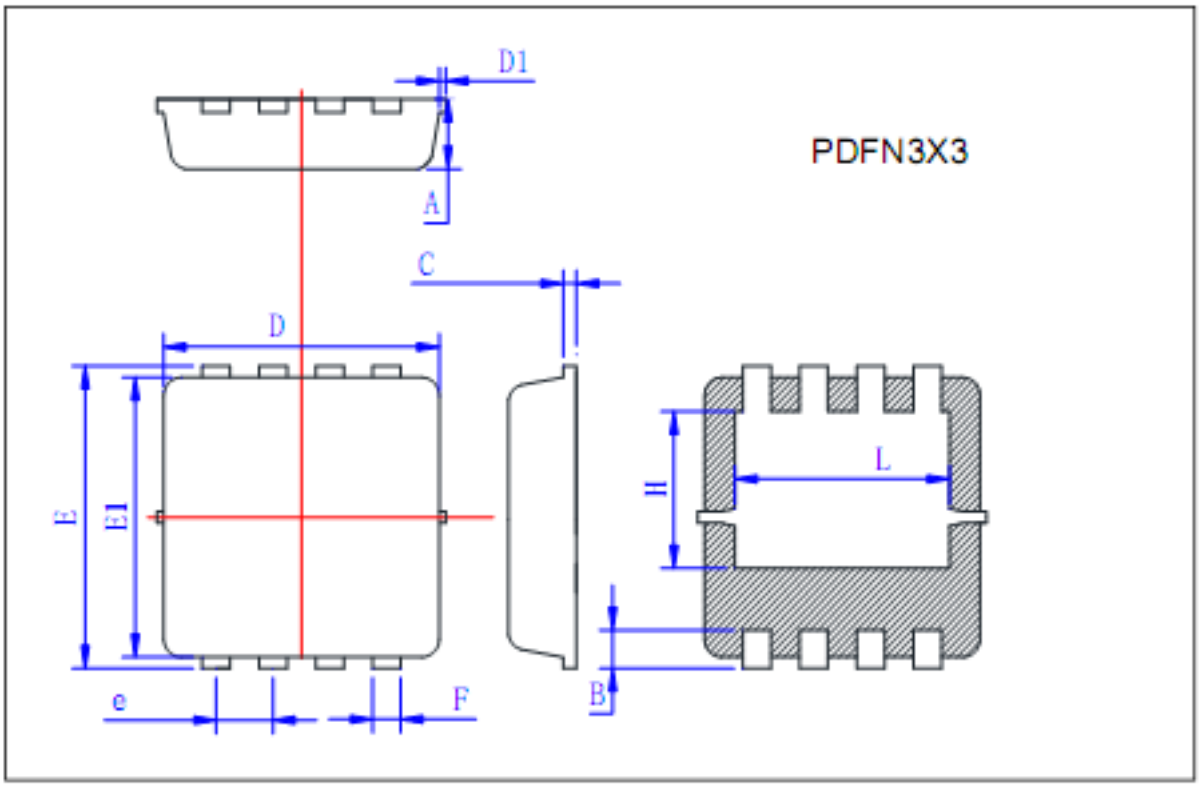


Figure 11 Normalized Maximum Transient Thermal Impedance

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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