

MT34P50/B/S

P-Channel Low Qg MOSFET

- 40V,-50A,17mΩ

Features

- $R_{DS(on)}=17m\Omega$ at $V_{GS} = -10V, I_D = -12A$
- High performance trench technology for extremely low $R_{DS(on)}$
- Low Gate Charge
- High power and current handing capability

General Description

This P-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

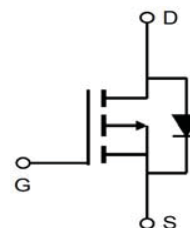
- DC-DC primary bridge
- DC-DC Synchronous rectification
- Power Managemement for Inverter Systems



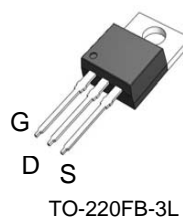
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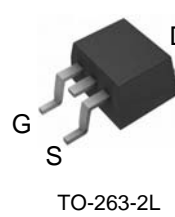
Simplified Schematic



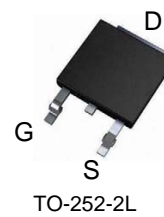
MARKING DIAGRAM & PIN ASSIGNMENT



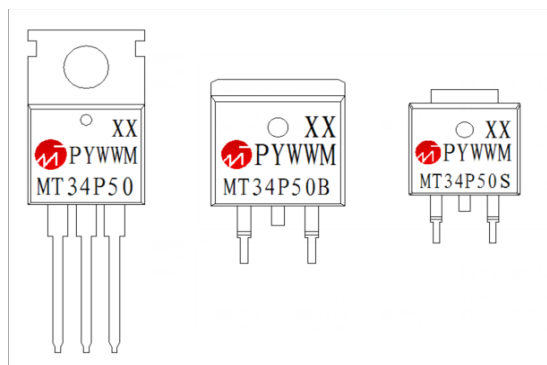
TO-220FB-3L



TO-263-2L



TO-252-2L



Package Code

MT34P50: T0-220FB-3L

MT34P50B: T0-263-2L

MT34P50S: T0-252-2L

Date Code Lot No

PYWWM

XX

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-50	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	-25	A
Pulsed Drain Current	I_{DM}	-160	A
Maximum Power Dissipation	P_D	80	W
Single pulse avalanche energy (Note 5)	E_{AS}	212	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.88	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

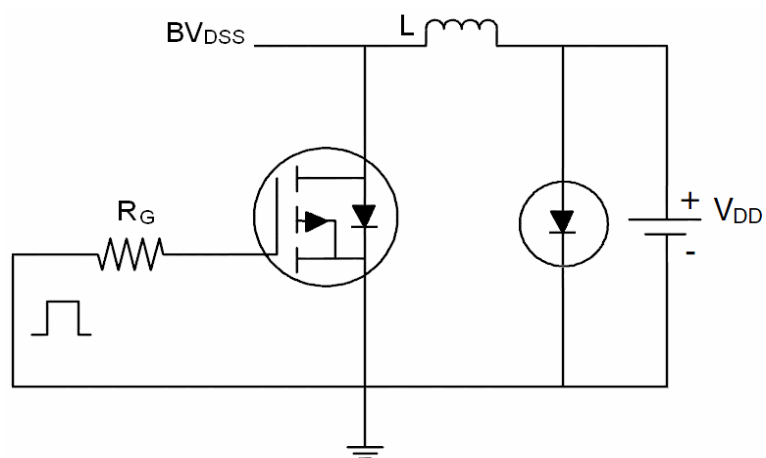
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1.5	-1.9	-3.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-12A	-	17	19	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-12A	34	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =-20V,V _{GS} =0V, F=1.0MHz	-	2960	-	PF
Output Capacitance	C _{oss}		-	370	-	PF
Reverse Transfer Capacitance	C _{rss}		-	310	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V,I _D =-20A V _{GS} =-10V,R _G =3Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	24	-	nS
Total Gate Charge	Q _g	V _{DS} =-20,I _D =-12A, V _{GS} =-10V	-	72		nC
Gate-Source Charge	Q _{gs}		-	14		nC
Gate-Drain Charge	Q _{gd}		-	15		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =-20A	-		-1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-50	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =- 20A di/dt = -100A/μs ^(Note3)	-	40		nS
Reverse Recovery Charge	Q _{rr}		-	42		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

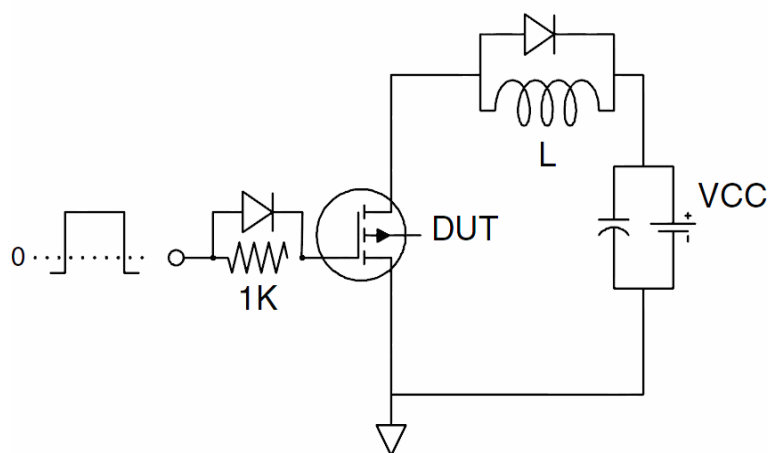
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_G=25\Omega, I_{AS}=33A$

Test Circuit

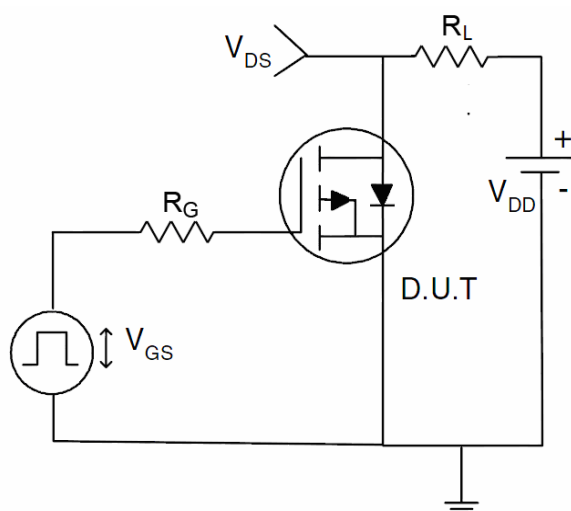
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

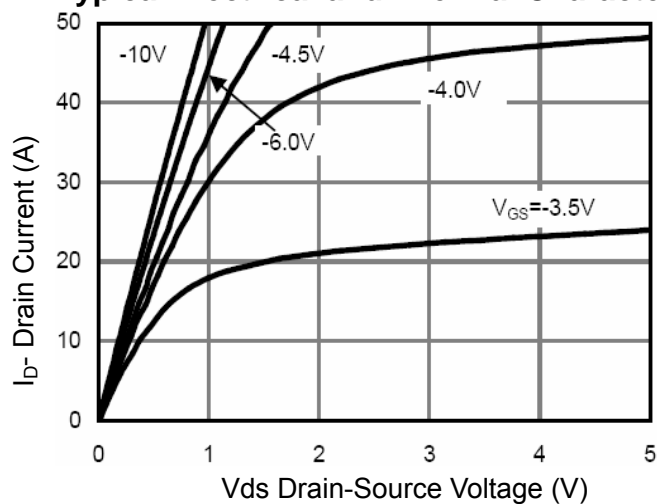


Figure 1 Output Characteristics

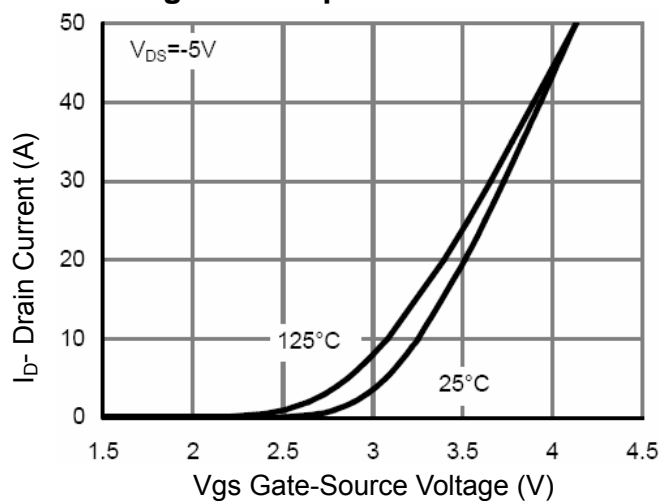


Figure 2 Transfer Characteristics

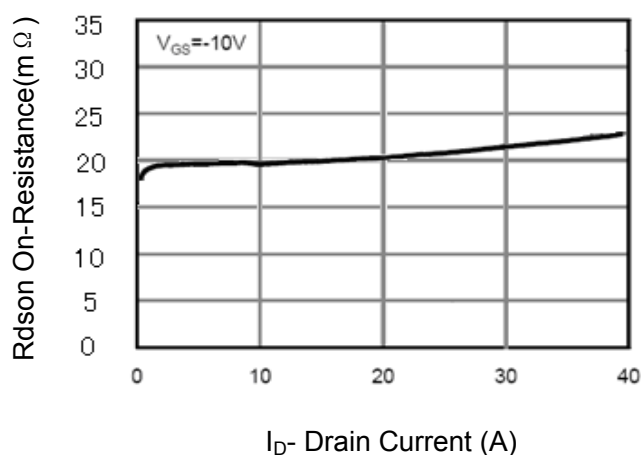


Figure 3 Rdson- Drain Current

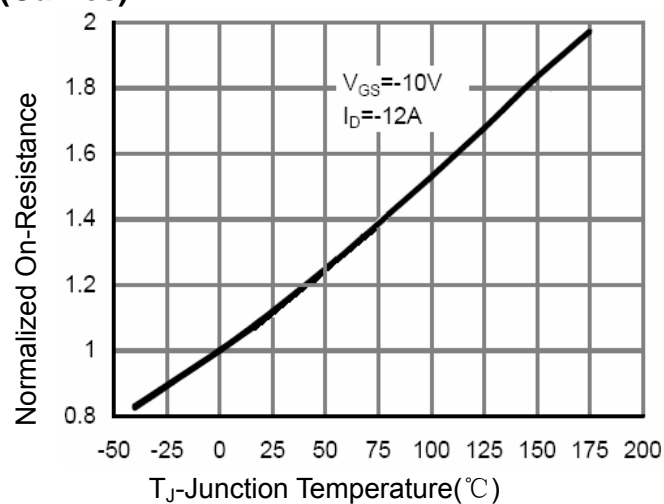


Figure 4 Rdson-Junction Temperature

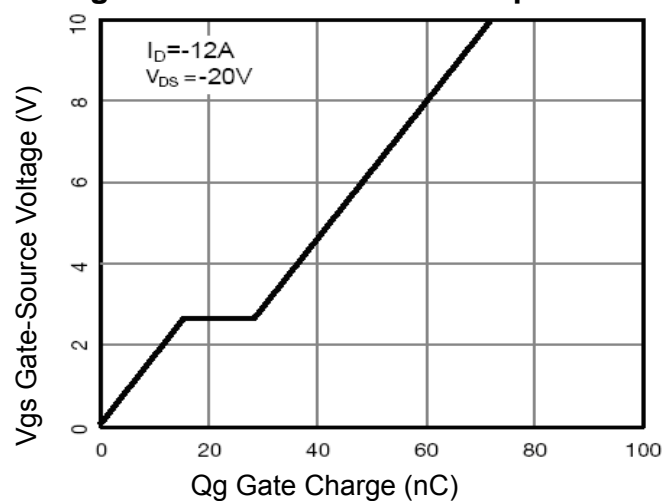


Figure 5 Gate Charge

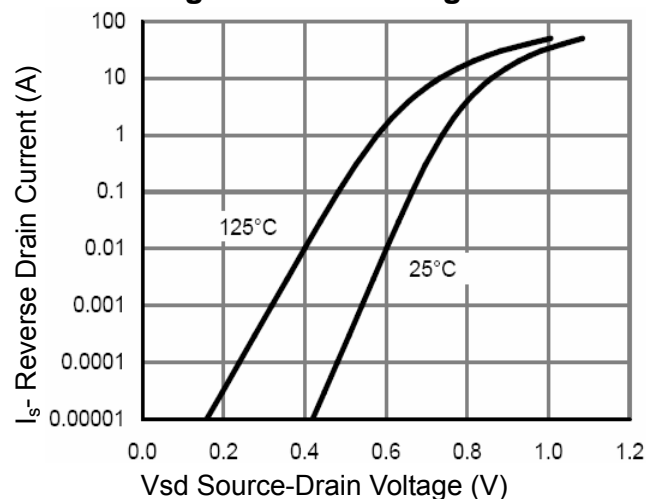


Figure 6 Source- Drain Diode Forward

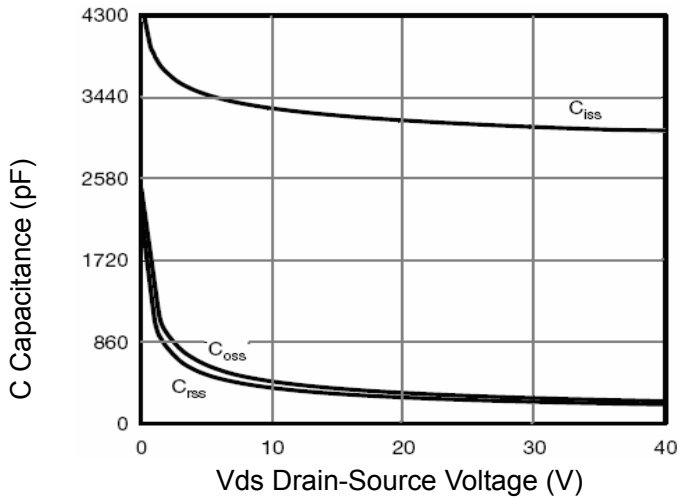


Figure 7 Capacitance vs Vds

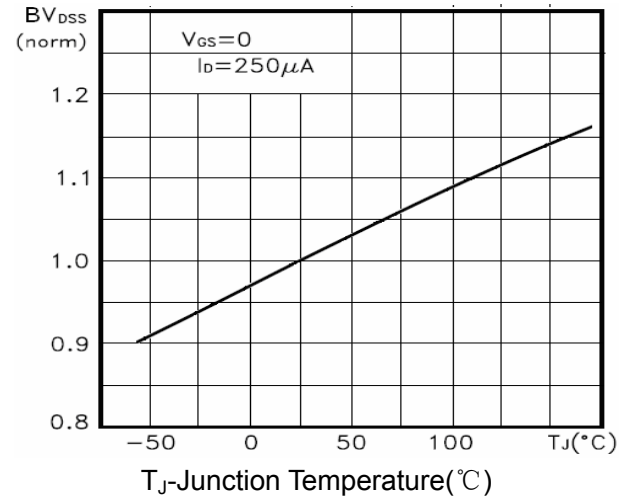
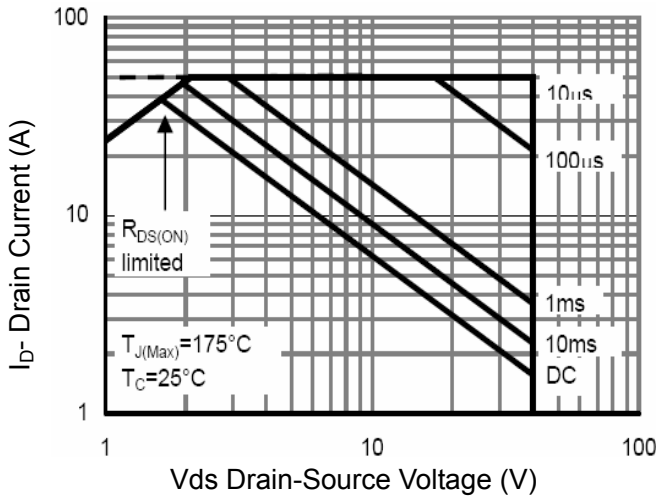
Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

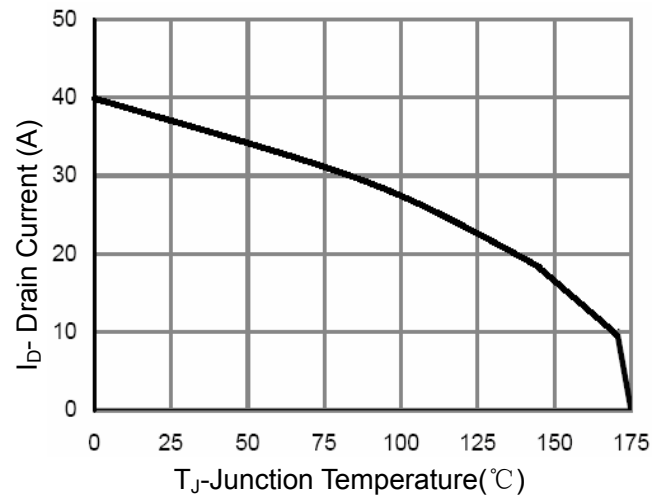
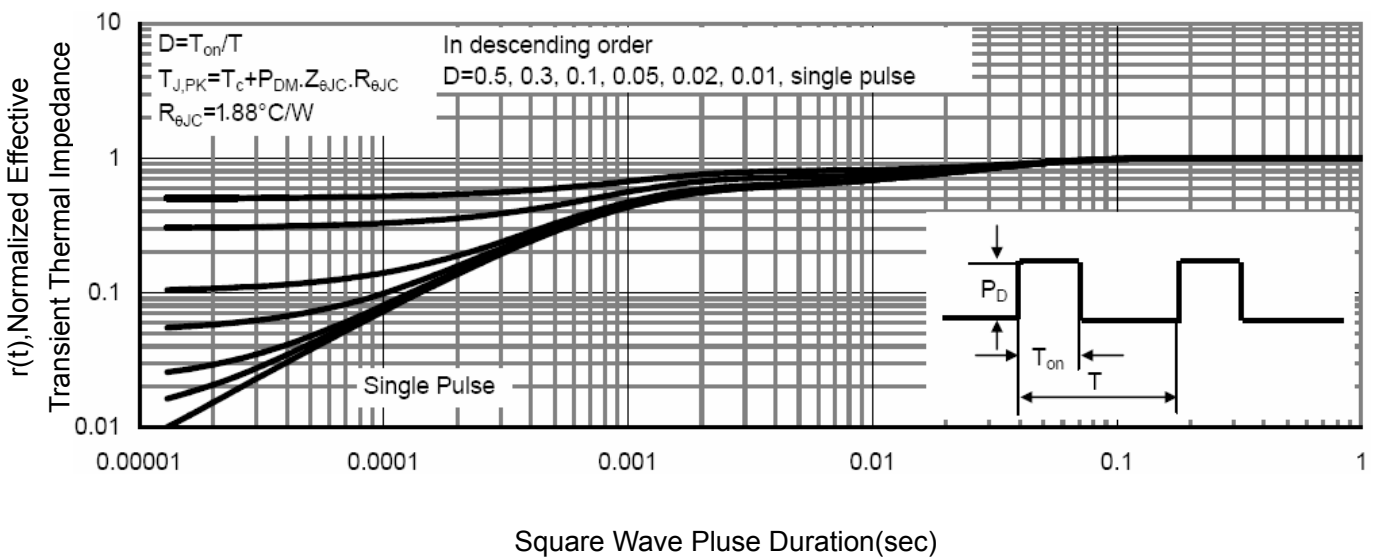
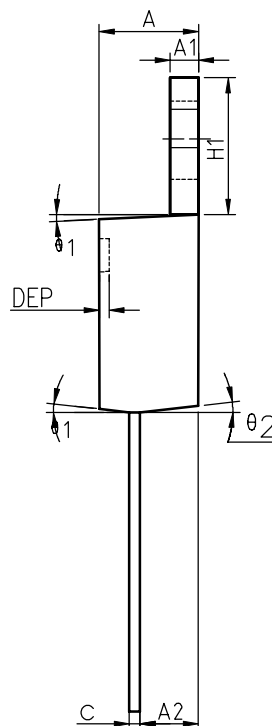
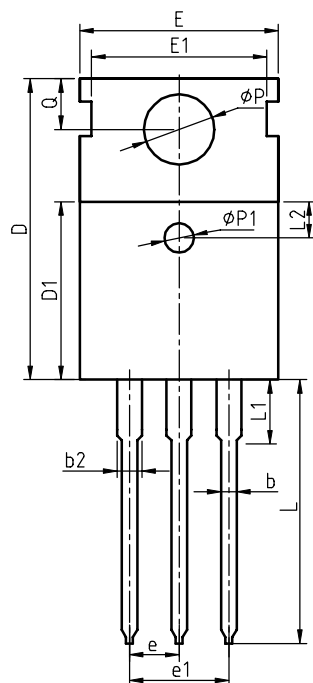
Figure 10 I_D Current Derating vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

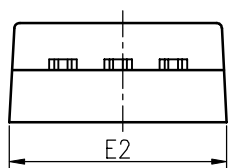
Package Information

TO-220FB-3L

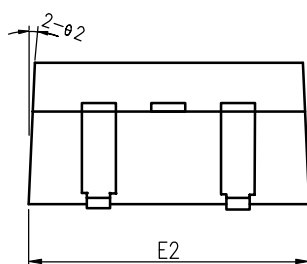
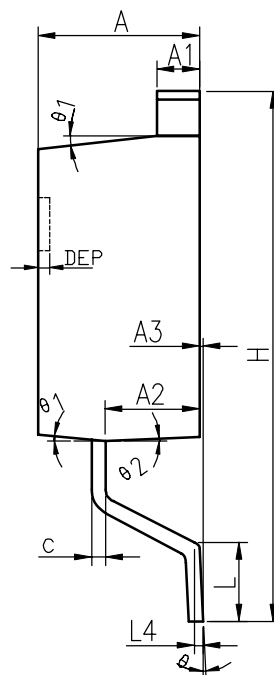
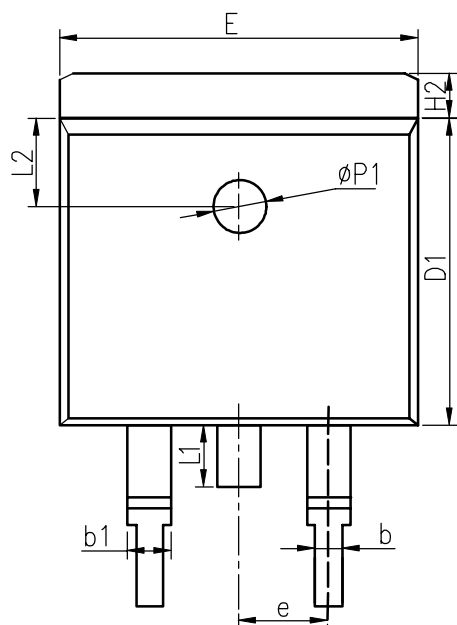


COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	—	8.70	—	—	0.343	—
E2	9.80	10.00	10.20	0.386	0.394	0.402
e	—	2.54	BSC	—	0.100	BSC
e1	—	5.08	BSC	—	0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	—	3.10	3.30	—	0.122	0.130
L2	—	2.50	REF	—	0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ 1	5°	7°	9°	5°	7°	9°
θ 2	1°	3°	5°	1°	3°	5°
θ 3	1°	3°	5°	1°	3°	5°



TO-263-2L



COMMON DIMENSIONS

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.22	1.27	1.32	0.048	0.050	0.052
A2	2.59	2.69	2.79	0.102	0.106	0.110
A3	0.00	0.10	0.20	0.000	0.004	0.008
b	0.77	0.813	0.90	0.030	0.032	0.035
b1	1.20	1.270	1.36	0.047	0.050	0.054
c	0.34	0.381	0.47	0.013	0.015	0.019
D1	8.60	8.70	8.80	0.339	0.343	0.346
E	10.00	10.16	10.26	0.394	0.400	0.404
E2	10.00	10.10	10.20	0.394	0.398	0.402
e	2.54 BSC			0.100 BSC		
H	14.70	15.10	15.50	0.579	0.594	0.610
H2	1.17	1.27	1.40	0.046	0.050	0.055
L	2.00	2.30	2.60	0.079	0.091	0.102
L1	1.45	1.55	1.70	0.057	0.061	0.067
L2	2.50 REF			0.098 REF		
L4	0.25 BSC			0.010 BSC		
	0°	5°	8°	0°	5°	8°
1	5°	7°	9°	5°	7°	9°
2	1°	3°	5°	1°	3°	5°
ΦP1	1.40	1.50	1.60	0.055	0.059	0.063
DEP	0.05	0.10	0.20	0.002	0.004	0.008

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.