MT3906S5

60V Complementary Power MOSFET

Features

 N-Channel 60V/8.0A,

 $R_{\text{DS}}(\text{ON}) = 36m_{\Omega} \text{ @ VGS} = 10V$

 $R_{DS}(ON) = 42m\Omega$ @ VGS = 4.5V

 P-Channel -60V/-6.0A.

 R_{DS} (ON) = $65m\Omega$ @ VGS = -10V

 $R_{DS}(ON) = 75m\Omega$ @ VGS = -4.5V

RoHS Compliant

General Description

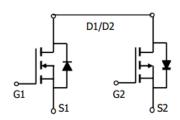
This complementary MOSFET device is produced using Mos-tech's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- · DC-DC converter
- Power management
- LCD backlight inverter
- DC-FAN

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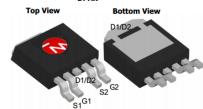


N-channel

P-channel

MARKING DIAGRAM & PIN ASSIGNMENT

TO252-4L DPAK



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	N-CH	P-CH	Units	
V _{DSS}	Drain-Source Voltage	60	-60	V	
V _{GSS}	Gate-Source Voltage	±20	±20	V	
1_	Drain Current - Continuous (Note 1a)	8.0	-6.0	А	
I _D	- Pulsed	25	-25		
P_D	Power Dissipation for Dual Operation	15	10	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to	°C		

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	62.5	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	41	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT3906S5	MT3906S5	-	-	2500 units

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Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
 Drain-Soເ	ırce Avalanche Rating	S (Note 1)					
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30 \text{ V}, \qquad I_D = 4.5 \text{ A}$	N-CH	-	-	93	mJ
I _{AR}	Maximum Drain-Source Avalanche Current		N-CH	-	-	7.0	Α
Off Chara	ecteristics	<u>.</u>			•	•	
BV _{DSS}	Drain-Source Breakdown	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	N-CH	60	_	_	V
ΔBVDSS	Voltage Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$ $I_{D} = 250 \mu\text{A}, \text{ Referenced to } 25^{\circ}\text{C}$	P-CH N-CH	-60	59		•
ΔD V DSS ΔT _J	Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25 °C	P-CH	-	-47	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain	V _{DS} = 48 V, V _{GS} = 0 V	N-CH	_	_	1	μА
	Current	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$	P-CH			-1	μ,
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	N-CH P-CH	-	-	<u>+</u> 100 <u>+</u> 100	nA
On Chara	cteristics (Note 2)						
	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	N-CH	1	2.0	3	V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-CH	-1	-2.0	-3	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C I_D = -250 μ A, Referenced to 25°C	N-CH P-CH	-	-5.6 4	-	mV/°C
ΔIJ	Tomporataro Goomolorit	$V_{GS} = 10 \text{ V}, I_{D} = 5.3 \text{A}$	1 -011		36	40	
		$V_{GS} = 10 \text{ V}, I_{D} = 5.3 \text{A}, T_{J} = 125^{\circ}\text{C}$	N-CH	-	52	64	
R _{DS(on)}	Static Drain-Source	$V_{GS} = 4.5 \text{ V}, I_D = 4.7 \text{A}$			42	45	mΩ
TUS(on)	On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -5.3\text{A}$		_	65	70	
		$V_{GS} = -10 \text{ V}, I_D = -5.3 \text{A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = -4.5 \text{ V}, I_D = -4.7 \text{A}$	P-CH		90 75	100 80	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	N-CH	20	-	_	A
-D(OII)	On-State Drain Current	$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	P-CH	-20			
g _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 5.3 \text{A}$ $V_{DS} = -5 \text{ V}, I_{D} = 5.3 \text{A}$	N-CH P-CH	-	6	-	S
Dynamic	Characteristics						
C _{iss}	Input Capacitance	N-CH	N-CH	-	680	-	pF
		$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $V_{DS} = 1.0 \text{ MHz}$	P-CH N-CH		770 86		<u> </u>
	Output Capacitance	P-CH	P-CH	-	94	-	pF
Urcc	Reverse Transfer Capacitance	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz	N-CH P-CH	-	37 39	-	pF
	Characteristics (Note 2)	1					
	urn-On Delay Time	N-CH	N-CH		13	23	ns
` '	•	$V_{DD} = 30 \text{ V}, I_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	P-CH N-CH		7	17 19	
	urn-On Rise Time	P-CH	P-CH	-	12	23	ns
d(off)	urn-Off Delay Time	$V_{DD} = -30 \text{ V}, I_{D} = -1 \text{ A},$	N-CH P-CH	-	19 19	39 37	ns
f T	urn-Off Fall Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	N-CH P-CH	-	6 12	17 25	ns
Q _g T	otal Gate Charge	N-CH V _{DS} = 30 V, I _D = 5.3A , V _{GS} = 10 V	N-CH P-CH	-	15.5 18	19 24	nC
Q _{gs}	Sate-Source Charge	P-CH	N-CH P-CH	-	2.6 2.7	-	nC
Q_{gd}	Sate-Drain Charge	$V_{DS} = -30 \text{ V}, I_D = -5.3 \text{A}, V_{GS} = -10 \text{V}$	N-CH P-CH	-	2.7	-	nC

-1.2

-0.8

P-CH

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted Symbol **Parameter** Min Тур Max Units **Test Conditions Type Drain-Source Diode Characteristics and Maximum Ratings** Maximum Continuous Drain-Source Diode Forward Current N-CH 1.4 Α -1.4 P-CH N-CH 0.8 1.2 $V_{\text{SD}} \\$ ٧

Scale 1 : 1 on letter size paper

Voltage

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^{1.} R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

^{2.} Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

Typical Characteristics: P-CH

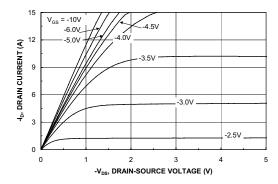


Figure 1. On-Region Characteristics.

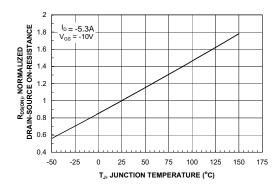


Figure 3. On-Resistance Variation with Temperature.

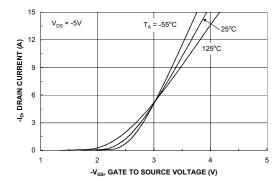


Figure 5. Transfer Characteristics.

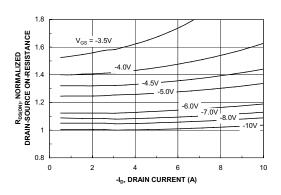


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

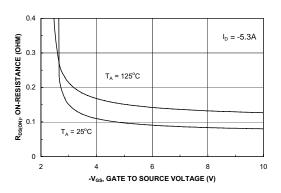


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

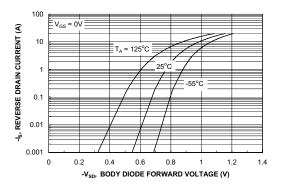


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-CH

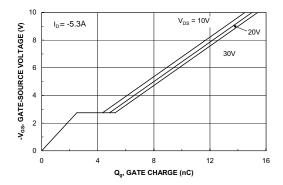


Figure 7. Gate Charge Characteristics.

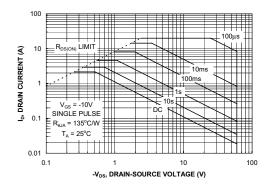


Figure 9. Maximum Safe Operating Area.

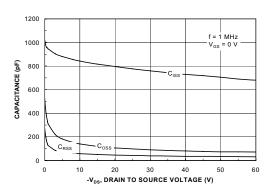


Figure 8. Capacitance Characteristics.

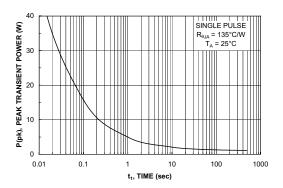


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N-CH

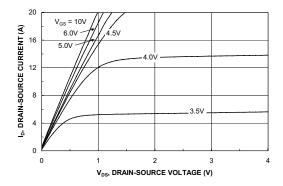


Figure 11. On-Region Characteristics.

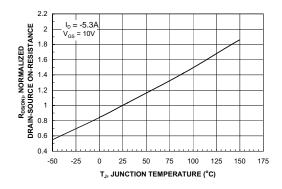


Figure 13. On-Resistance Variation with Temperature.

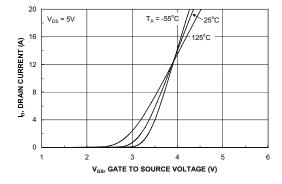


Figure 15. Transfer Characteristics.

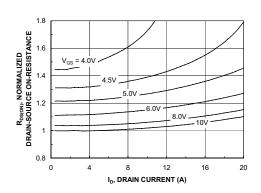


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

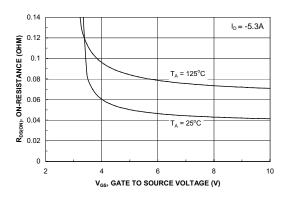


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

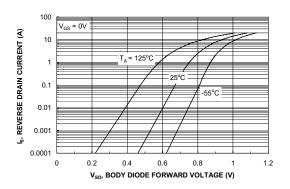
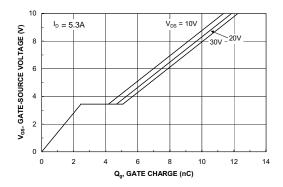


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-CH



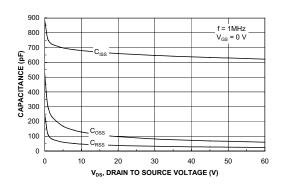


Figure 17. Gate Charge Characteristics.

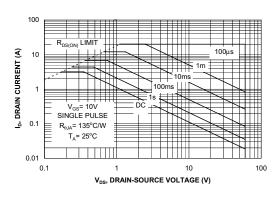


Figure 18. Capacitance Characteristics.

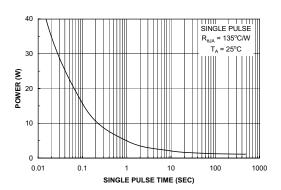


Figure 19. Maximum Safe Operating Area.



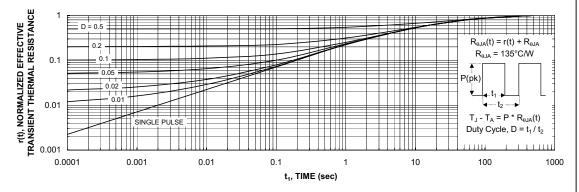
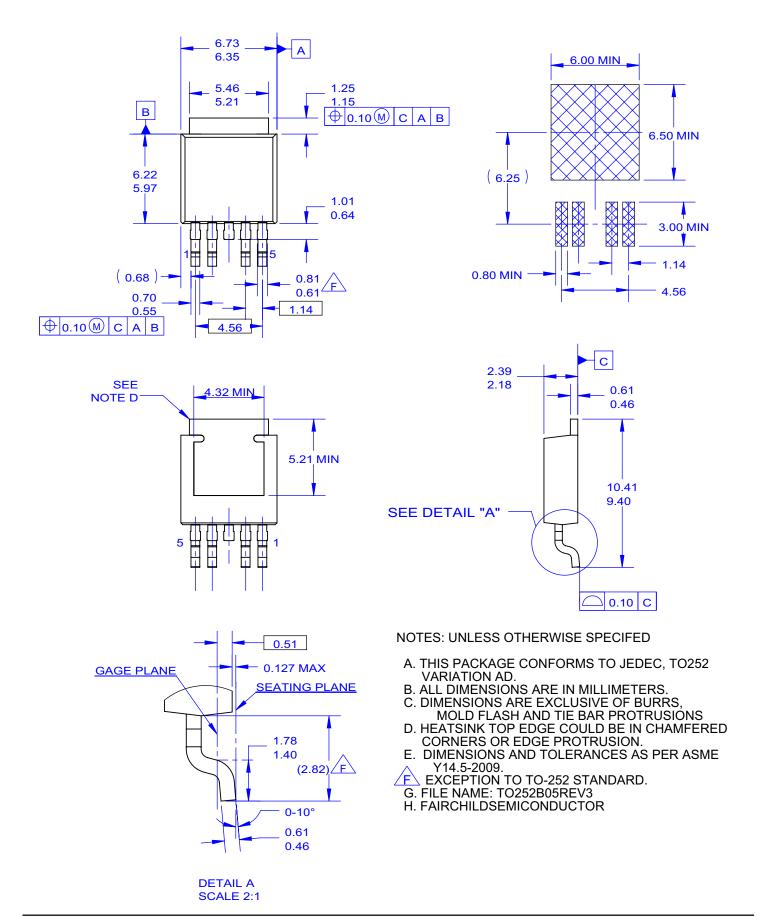


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



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