

MT4235

40V Complementary Power MOSFET

Features

- N-Channel
40V/4.5A
 $R_{DS(ON)} = 26m\Omega$ (typ) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 35m\Omega$ (typ) @ $V_{GS} = 4.5V$
- P-Channel
-40V/-4.0A
 $R_{DS(ON)} = 64m\Omega$ (typ) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 85m\Omega$ (typ) @ $V_{GS} = -4.5V$
- RoHS Compliant

General Description

This complementary MOSFET device is produced using Mos-tech's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC-DC converter
- Power management
- LCD backlight inverter

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-CH	P-CH	Units
V _{DSS}	Drain-Source Voltage	40	-40	V
V _{GSS}	Gate-Source Voltage	± 20	± 20	V
I _D	Drain Current - Continuous			

Thermal Characteristics

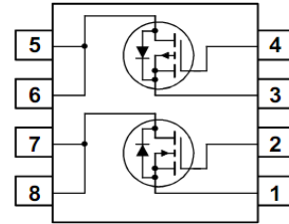
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	75	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	45	$^\circ\text{C/W}$



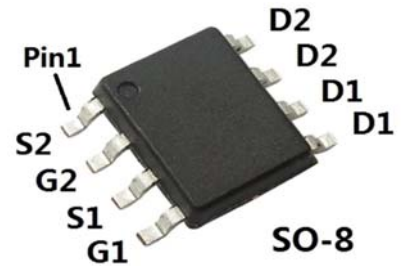
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA V _{GS} = 0 V, I _D = -250 μA	N-CH P-CH	40 -40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	N-CH P-CH	-	21 -13	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40V, V _{GS} = 0 V V _{DS} = -40V, V _{GS} = 0 V	N-CH P-CH	-	-	1 -1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±20 V, V _{DS} = 0 V V _{GS} = ±20 V, V _{DS} = 0 V	N-CH P-CH	-	-	±100 ±100	nA

On Characteristics (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA V _{DS} = V _{GS} , I _D = -250 μA	N-CH P-CH	1 -1	1.6 -1.7	2.0 -2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	N-CH P-CH	-	-3.6 -3.6	-	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 3.0A V _{GS} = 4.5V, I _D = 2.5A	N-CH	- -	26 35	36 50	mΩ
		V _{GS} = -10V, I _D = -1.2A V _{GS} = -4.5V, I _D = -1.0A	P-CH	- -	64 85	85 115	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V V _{GS} = -10 V, V _{DS} = -5 V	N-CH P-CH	4.5 -4	-	-	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 4.5 A V _{DS} = -5 V, I _D = -3.5 A	N-CH P-CH	-	17 15	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	N-CH V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	N-CH P-CH	- -	350 70	-	pF
C _{oss}	Output Capacitance	P-CH	N-CH P-CH	- -	49 23	-	pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz	N-CH P-CH	- -	76 38	-	pF

Switching Characteristics (Note 2)

t _{d(on)}	Turn-On Delay Time	N-CH V _{DD} = 10 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 1 Ω	N-CH P-CH	- -	4 6	-	ns
t _r	Turn-On Rise Time		N-CH P-CH	- -	7.8 14	-	ns
t _{d(off)}	Turn-Off Delay Time	P-CH V _{DD} = -10 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 1 Ω	N-CH P-CH	- -	23 28	-	ns
t _f	Turn-Off Fall Time		N-CH P-CH	- -	8 13	-	ns
Q _g	Total Gate Charge	N-CH V _{DS} = 10 V, I _D = 4.5 A, V _{GS} = 10 V	N-CH P-CH	- -	14 11	-	nC
Q _{gs}	Gate-Source Charge	P-CH	N-CH P-CH	- -	1.2 0.9	-	nC
Q _{gd}	Gate-Drain Charge	V _{DS} = -10 V, I _D = -3.5 A, V _{GS} = -10V	N-CH P-CH	- -	2.5 1.9	-	nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

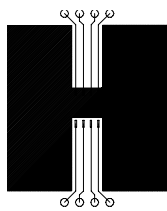
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Diode Characteristics and Maximum Ratings

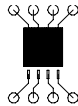
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-CH P-CH	-	-	1.4 -1.4	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -3.5\text{ A}$ (Note 2)	N-CH P-CH	-	0.8 -0.9	-	V

Notes:

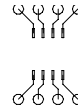
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$

TYPICAL CHARACTERISTICS P-CH

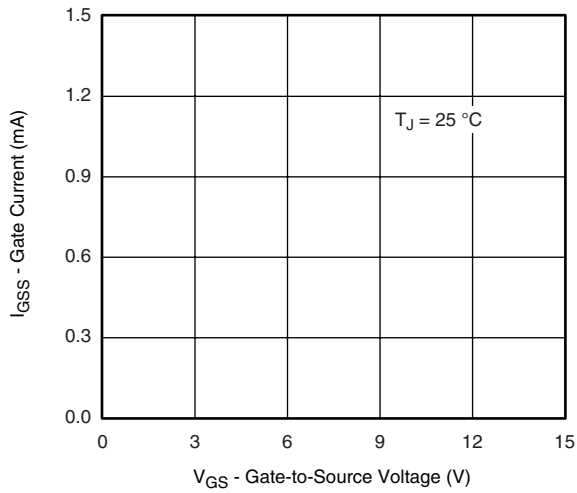


Figure 1 Gate Current vs. Gate-Source Voltage

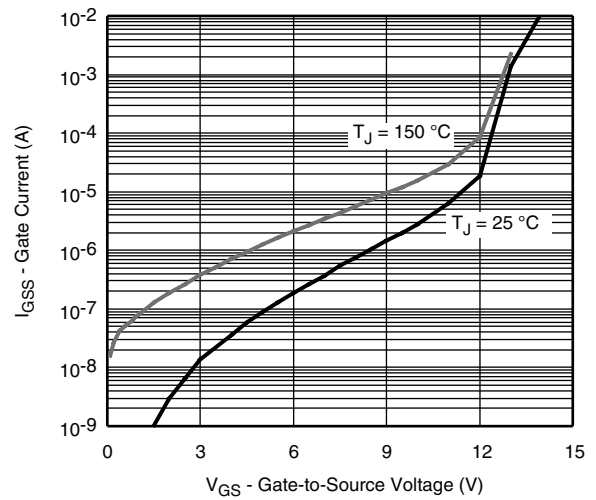


Figure 2 Gate Current vs. Gate-Source Voltage

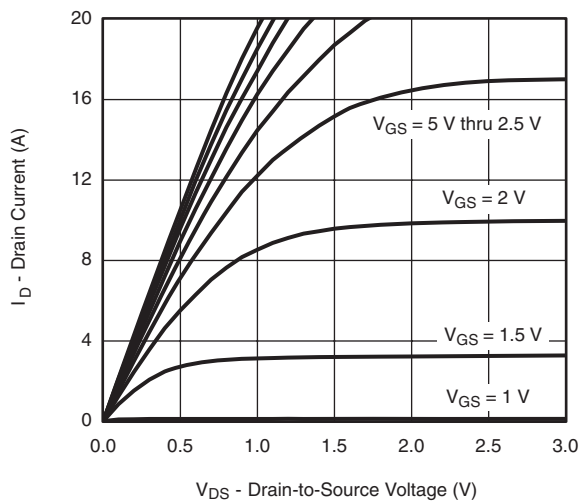


Figure 3 Output Characteristics

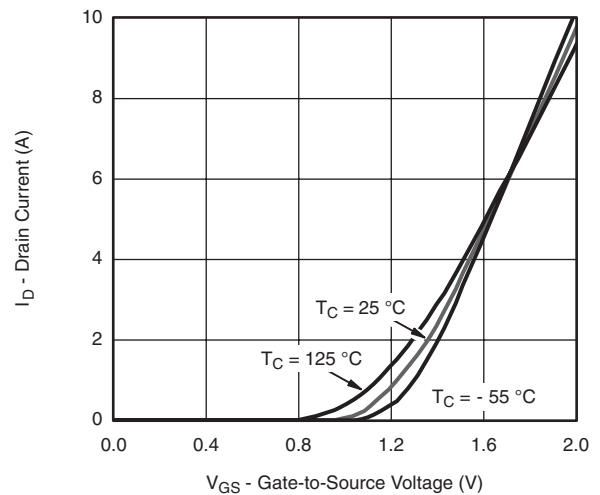


Figure 4 Transfer Characteristics

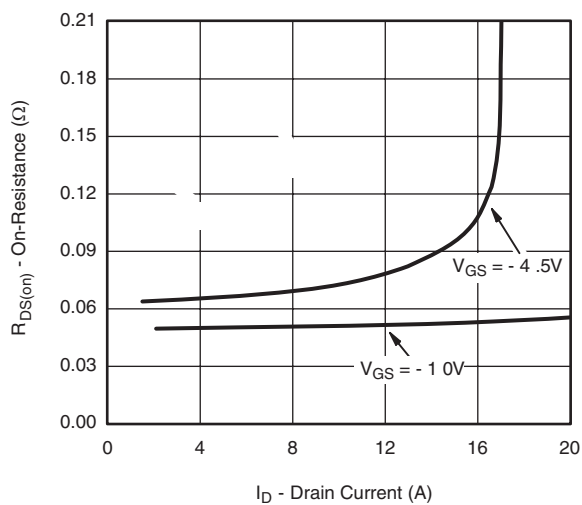


Figure 5 On-Resistance vs. Drain Current

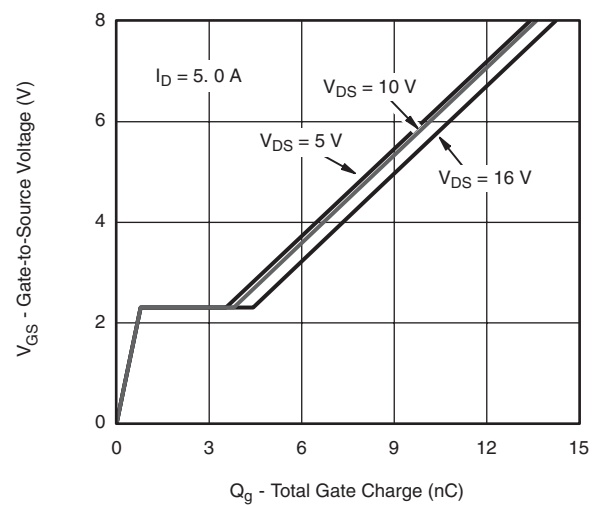


Figure 6 Gate Charge

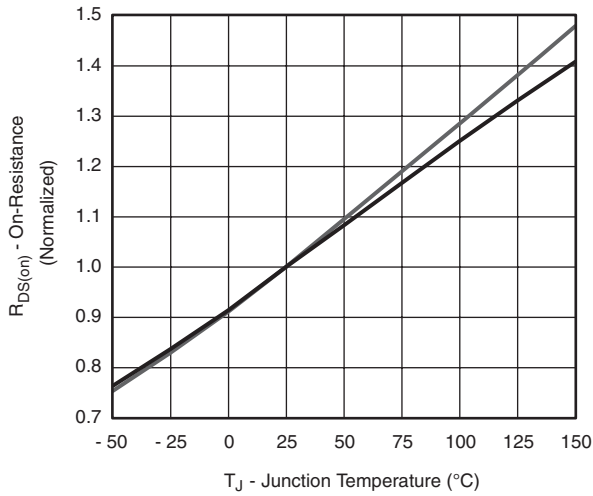


Figure 7 On-Resistance vs. Junction Temperature

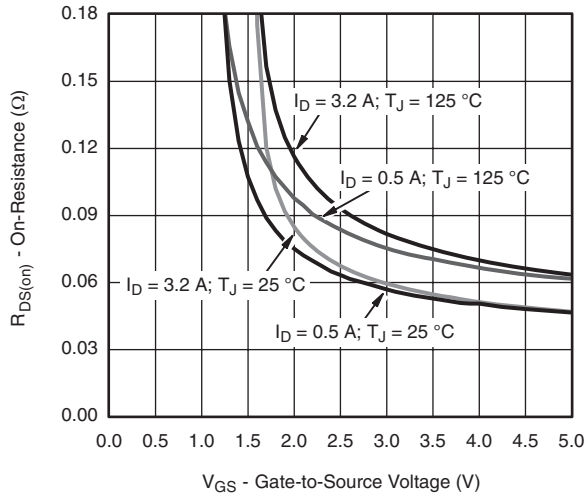


Figure 9 On-Resistance vs. Gate-to-Source Voltage

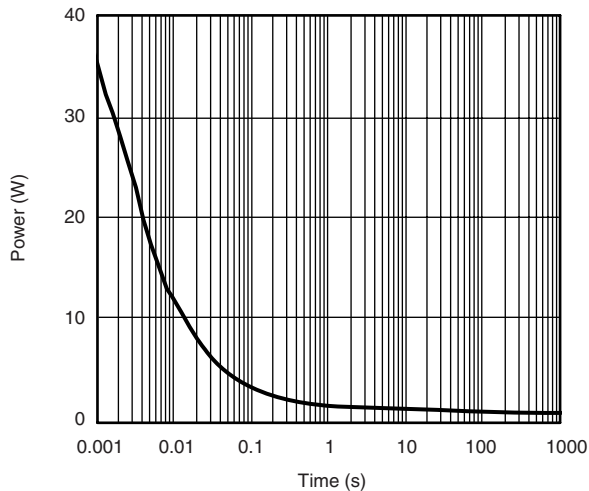


Figure 11 Single Pulse Power, Junction-to-Ambient

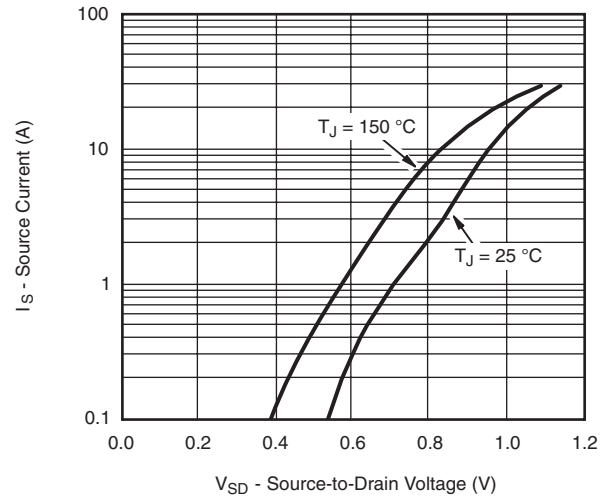


Figure 8 Source-Drain Diode Forward Voltage

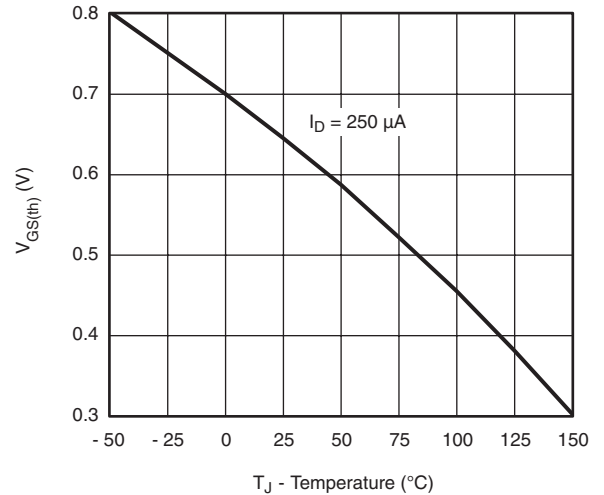


Figure 10 Threshold Voltage

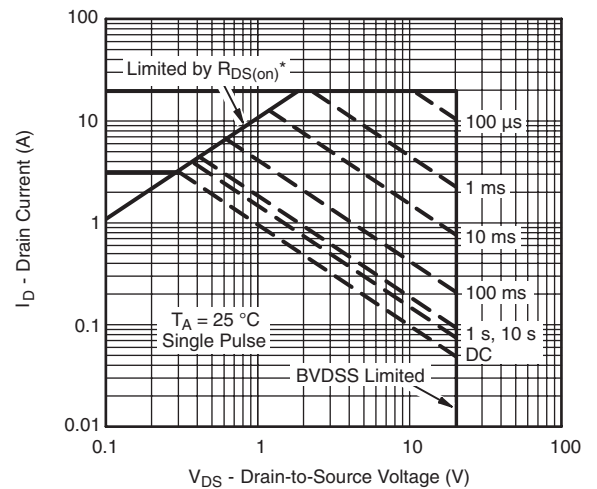


Figure 12 Safe Operating Area, Junction-to-Ambient

Typical Characteristics: N-CH

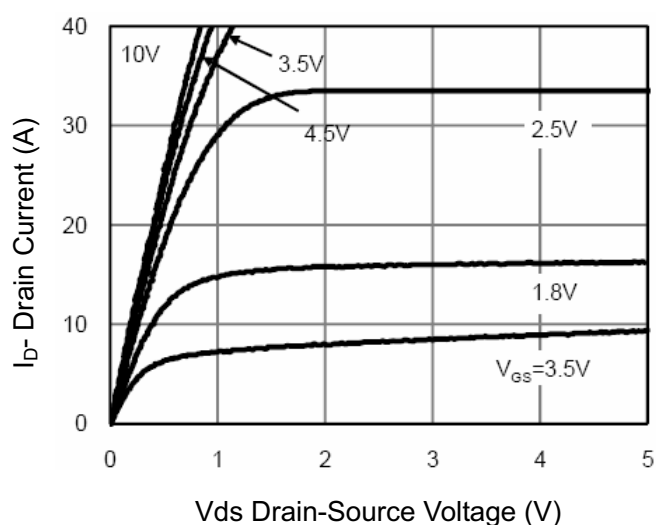


Figure 1 Output Characteristics

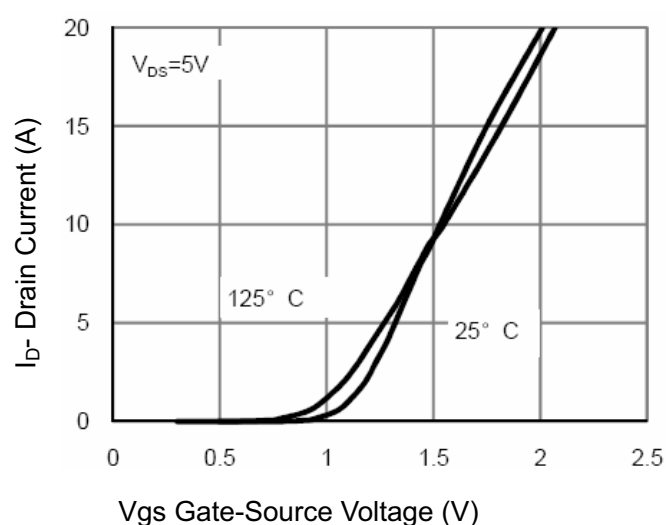


Figure 2 Transfer Characteristics

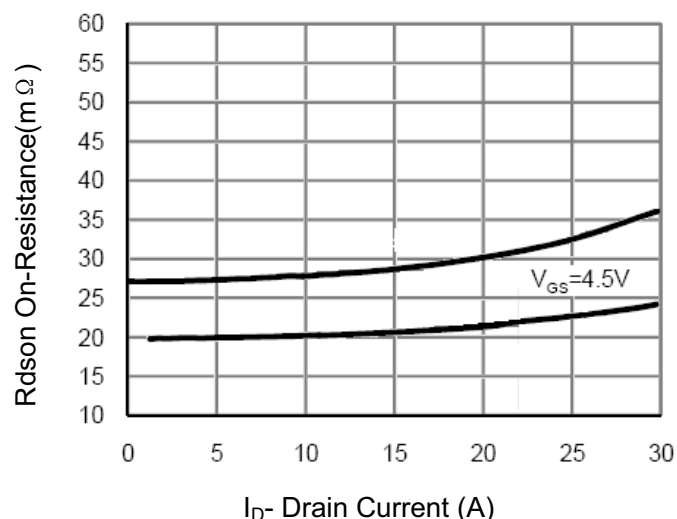


Figure 3 Drain-Source On-Resistance

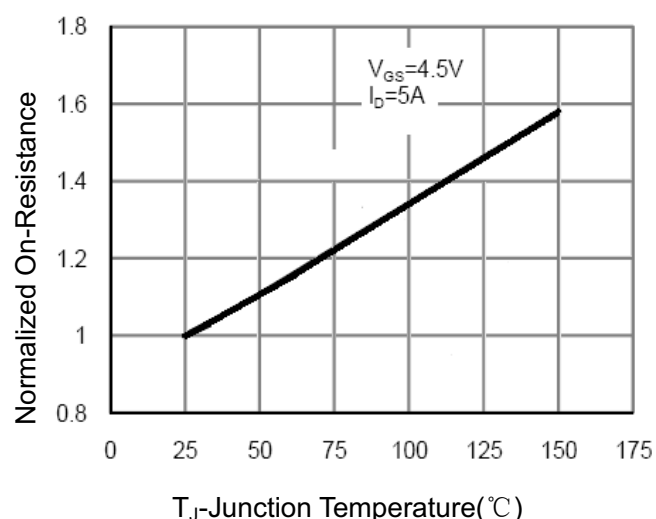


Figure 4 Drain-Source On-Resistance

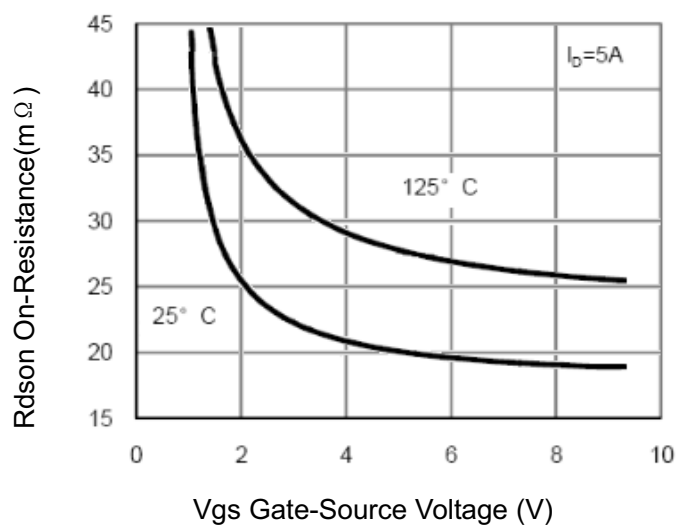
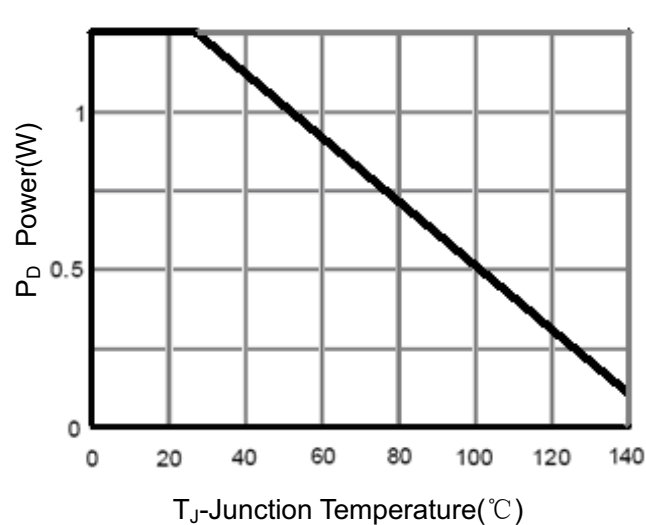


Figure 5 Rdson vs Vgs



Typical Characteristics: N-CH

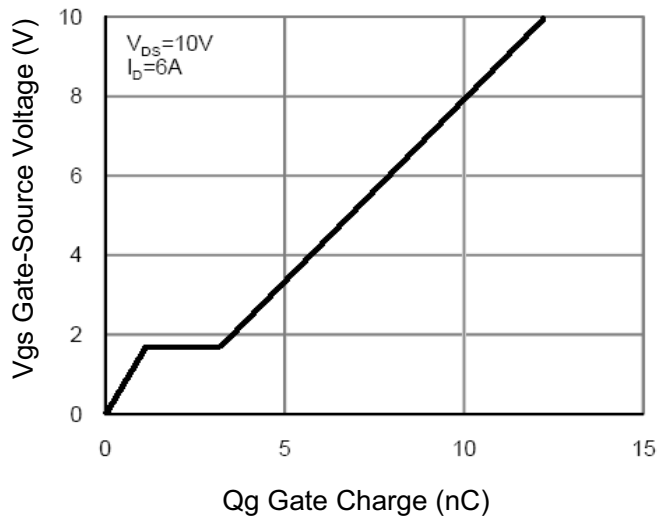


Figure 7 Gate Charge

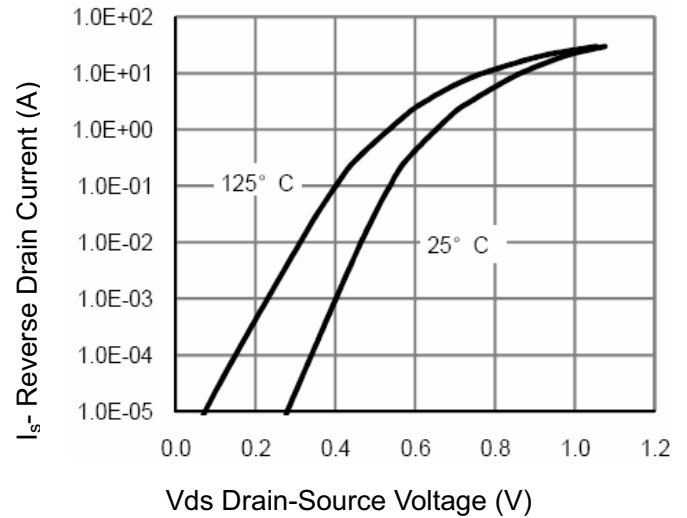


Figure 8 Source- Drain Diode Forward

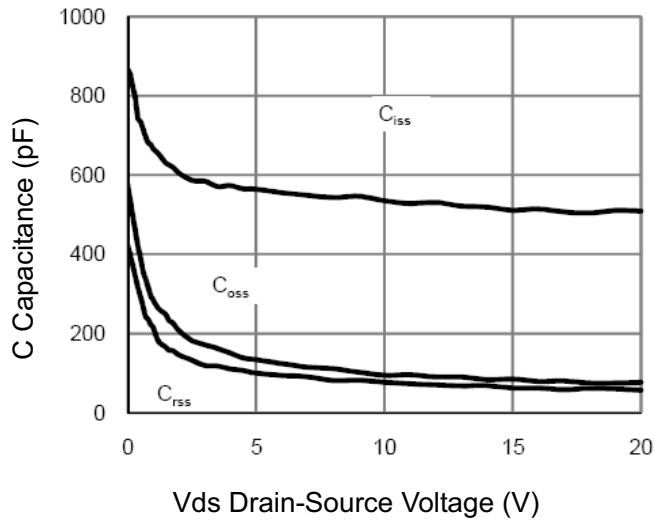


Figure 9 Capacitance vs Vds

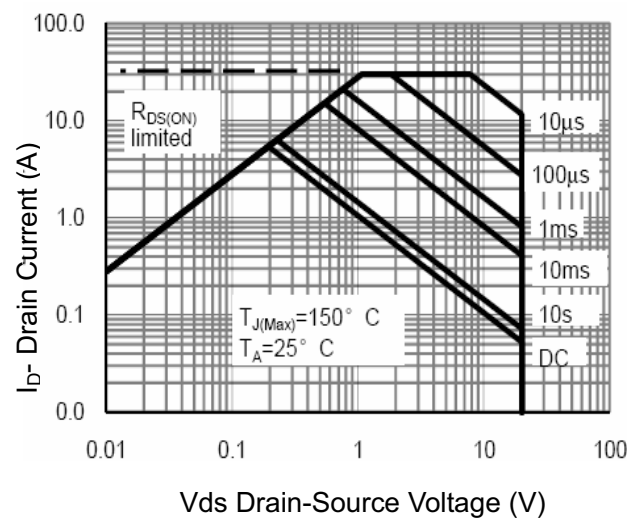


Figure 10 Safe Operation Area

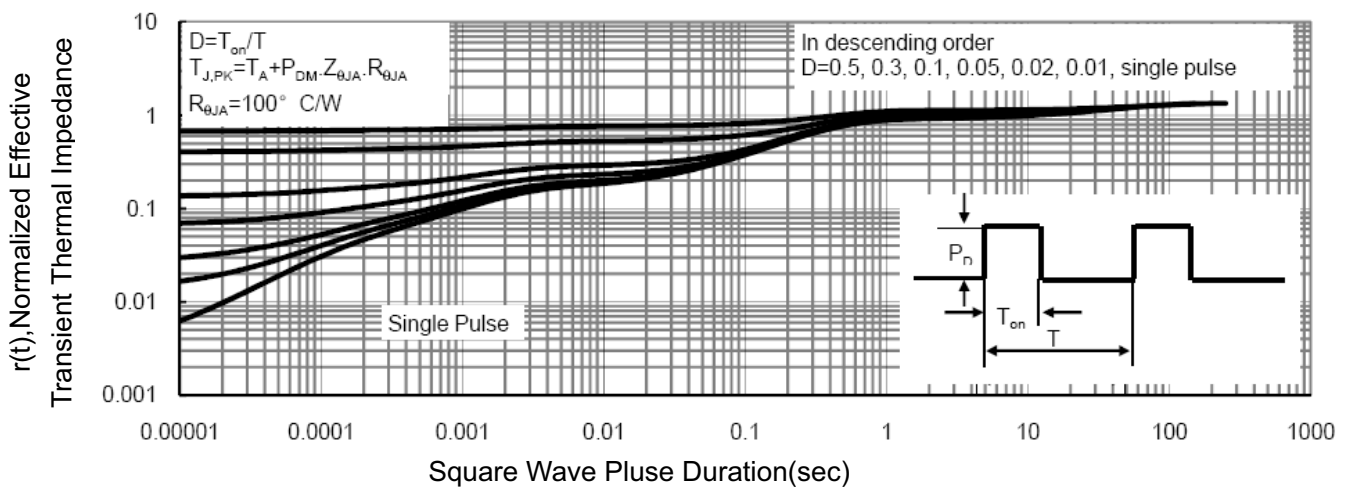
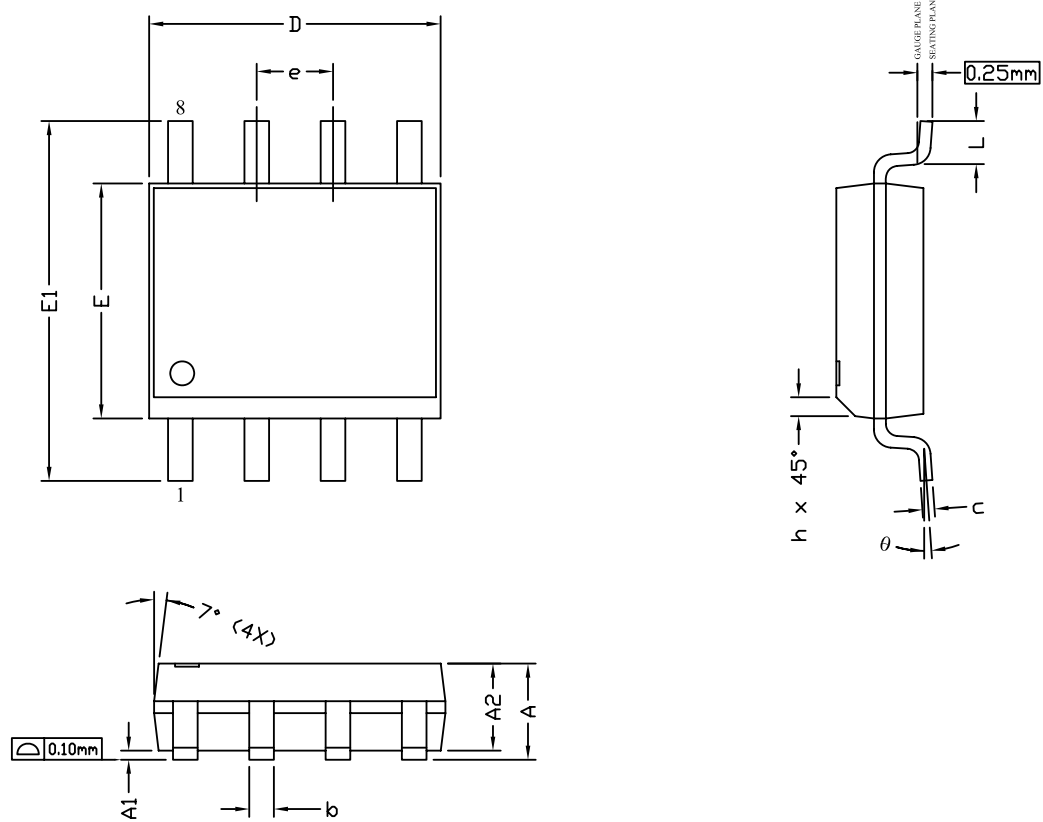


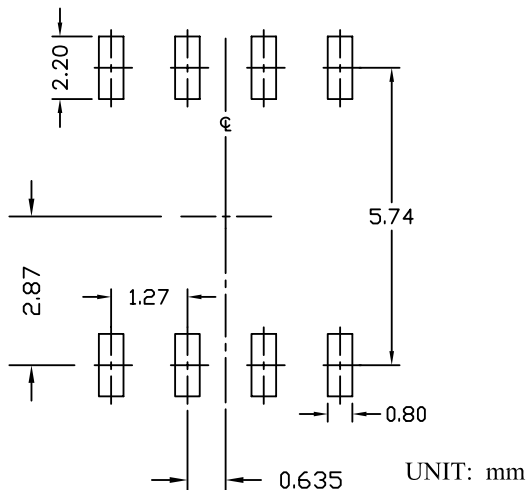
Figure 11 Normalized Maximum Transient Thermal Impedance

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Version	rev H

S08 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
θ	0°	—	8°	0°	—	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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 - 4) 其他直接影响到人的生命的装置。
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10. 本公司一直致力于提高产品的质量和可靠性, 但一般来说, 半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失, 希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等, 这是作为机器和系统的出厂保证。特别是单片机的软件, 由于单独进行验证很困难, 所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
11. 如果把本资料所记载的产品从其载体设备上卸下, 有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时, 请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时, 本公司将不承担任何责任。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.