MT4407

P-Channel MOSFET -30V, -12A, $13m\Omega$

General Description

This N-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

This device is well suited for Power Management and Load switching applications common in Notebook computers and Portable Battery Packs.

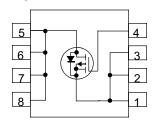
Features

- $R_{DS(on)} = 13m\Omega$ @ $V_{GS} = -10V$, $I_D = -12A$
- $R_{DS(on)} = 20 \text{m} \Omega @ V_{GS} = -4.5 \text{V}, I_D = -12 \text{A}$
- Extended V_{GS} range (-25V) for battery applications
- High performance trench technology for extremely low RDS(ON)
- · High power and current handling capability
- · RoHS compliant

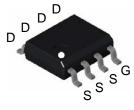


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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



SO-8

Absolute Maximum Ratings(T_A = 25 ℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V _{DS}	Drain to Source Voltage	-30	V
V _{GS}	Gate to Source Voltage	±20	V
	Drain Current -Continuous (Not	e1a) -12	Α
ID	-Pulsed	-75	Α
	Power Dissipation for Single Operation (No	te1a) 2.5	
P_{D}	(No	te1b) 1.2	W
	(No	te1c) 1.0	
T _J , T _{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
MT4407	MT4407	13"	12mm	2500 units

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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units

Off Characteristics

B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0V$	-30			V
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		-20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$			±100	nA

On Characteristics (Note 2)

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		8.1		mV/°C
	Drain to Source On Resistance	$V_{GS} = -10V$, $I_D = -12A$		13	15	
race s		$V_{GS} = -4.5V, I_D = -12A$		20	22	m_{Ω}
r _{DS(on)}		$V_{GS} = -10V, I_D = -12A$ $T_J = 125^{\circ}C$		17	22	11122
9 _{FS}	Forward Transconductance	$V_{DS} = -5V, I_{D} = -12A$		60		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 15V V - 0V	1200		pF
Coss	Output Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz	400		pF
C _{rss}	Reverse Transfer Capacitance	1 - 1.00012	160	190	pF

Switching Characteristics (Note 2)

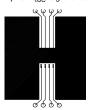
t _{d(on)}	Turn-On Delay Time		7		ns
t _r	Rise Time	$V_{DD} = -15V, I_{D} = -1A$ $V_{GS} = -10V, R_{GS} = 6\Omega$	9	12	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -10V, H_{GS} = 0.22$	25.6	28	ns
t _f	Fall Time		12	16	ns
Qg	Total Gate Charge	$V_{DS} = -15V, V_{GS} = -10V,$ $I_{D} = -12A$	88	124	nC
Qg	Total Gate Charge	V 45V V 5V	46	65	nC
Q _{gs}	Gate to Source Gate Charge	$V_{DS} = -15V, V_{GS} = -5V,$ $I_{D} = -12A$	8		nC
Q _{qd}	Gate to Drain Charge	ID12A	23.5		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = -2.1A$	-0.7	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = 12A, di/dt = 100A/μs		45	ns
Q _{rr}	Reverse Recovery Charge	I _F = 12A, di/dt = 100A/μs		34	nC

Notes:

1: R_{NJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) 50 °C/W (10 sec) when mounted on a 1 in² pad of 2 oz copper



b) 105 °C/W when mounted on a .04 in² pad of 2 oz copper





Scale 1: 1 on letter size paper

2: Pulse Test: Pulse Width < $300\mu s$, Duty Cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

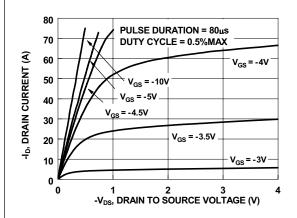
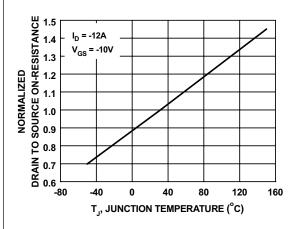


Figure 1. On Region Characteristics

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage



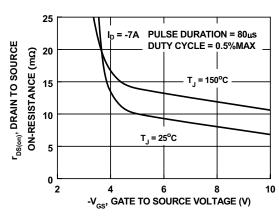
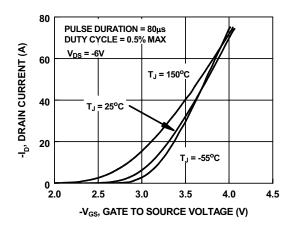


Figure 3. Normalized On Resistance vs Junction Temperature

Figure 4. On-Resistance vs Gate to Source Voltage



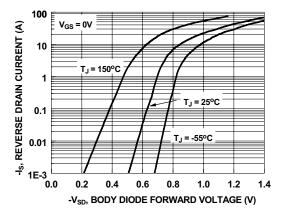


Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

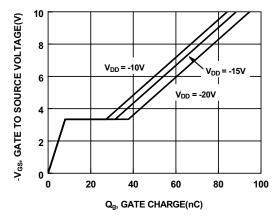


Figure 7. Gate Charge Characteristics

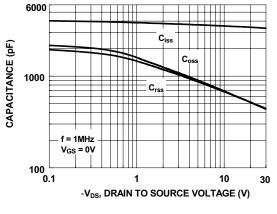


Figure 8. Capacitance vs Drain to Source Voltage

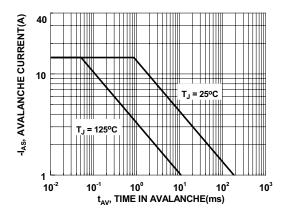


Figure 9. Unclamped Inductive Switching Capability

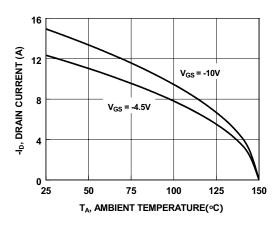


Figure 10. Maximum Continuous Drain Current vs
Ambient Temperature

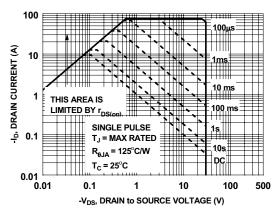


Figure 11. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unless otherwise noted

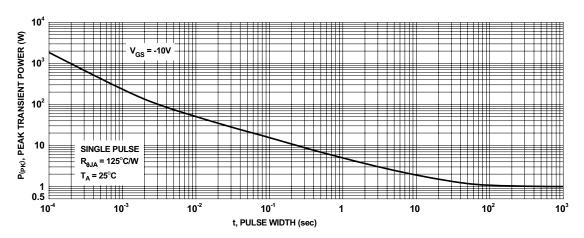


Figure 13. Single Pulse Maximum Power Dissipation

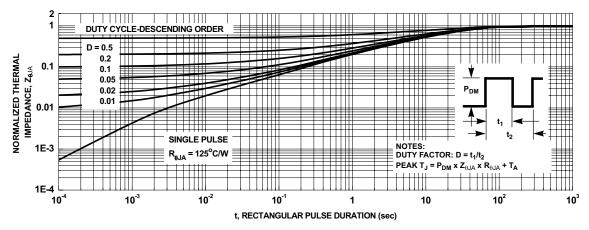
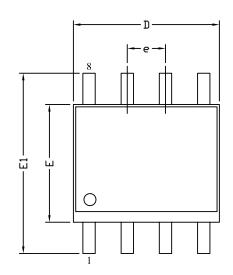


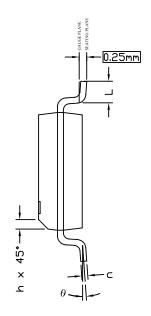
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

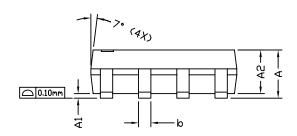
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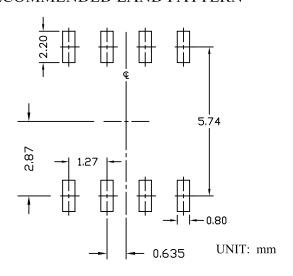
SO8 PACKAGE OUTLINE







RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIC	NS IN MILL	IMETERS	DIME	NSIONS IN IN	CHES
3 I MBOLS	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10		0.25	0.004		0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
Е	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			(0.050 BSC	7
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
θ	00		80	00		80

NOTE

- 1. ALL DIMENSIONS ARE IN MILLMETERS.
- 2. DIMENSIONS ARE INCLUSIVE OF PLATING.
- 3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- 4. DIMENSION L IS MEASURED IN GAUGE PLANE.
- 5. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

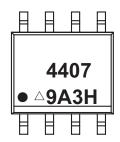
6

SOIC-8 Tape and Reel Data SOIC(8lds) Packaging Configuration: Figure 1.0 Packaging Description: Packaging Description: SOIC-8 parts are s hipped in tape. The c arrier tape is made f roma dissipative (carbon filled) polycarbonate reason. The cover tape is a multilayer film (rheat Activated Adhesive in nature) primarily composed of polyester film, adhesive la yer, s ealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13° or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 17° or 177cm diameter reel. This and s ome of ther options are further described in the Packaging information table. These full reels are in dividually ba roced is beled and AP Antistatic Cover Tape ESD Label These full reels are in dividually be roode la beled a nd placed in side a standard intermediate box (illustrated in figure 1.0) m ade of recyclable corrugated brown pa per. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped. Static Dissipative **Embossed Carrier Tape** ACTR Label SOIC (8lds) Packaging Information Packaging Option L86Z no flow code ACTR **SOIC-8 Unit Orientation** Packaging type 2,500 4,000 500 Qty per Reel/Tube/Bag Reel Size 13" Dia 13" Dia 7" Dia Box Dimension (mm) 343x64x343 530x130x83 343x64x343 184x187x47 5,000 30,000 8,000 1,000 Max qty per Box 0.0774 0.0774 0.0774 Weight per unit (gm) Weight per Reel (kg) 0.6060 0.9696 0.1182 Note/Comments 343mm x 342mm x 64mm Standard Intermediate box MT4407ACTR Label sample XH1 MT4407ACTR 2500 QTY: 2500 -MOS-TECH SEMICONDUCTOR LTD-SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0 \bigcirc 0 0 0 0 0 0 0 \bigcirc 0 0 0 0 \bigcirc 0 0 0 Components Trailer Tape Leader Tape 1680mm minimum or 640mm minimum or 80 empty pockets 210 empty pockets

Part Marking Information

SO-8 (PMG Code)

SO-8 Devices



4407 = Example Base Part Number

• = Pin 1 Indicator

△ = ESD Symbol 🖾

9 = Year Code

A = Month Code

3 = Week Code

H = Assembly Factory Code

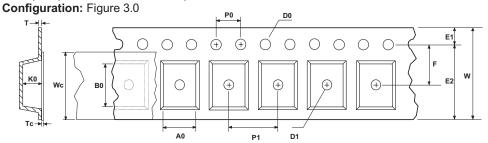
NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

SOIC-8 Tape and Reel Data, continued

SOIC(8lds) Embossed Carrier Tape



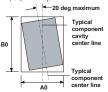
User Direction of Feed	

Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



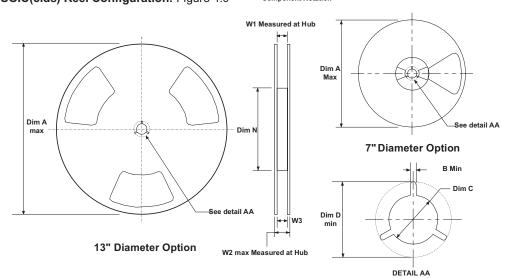
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters											
Tape Size	Reel Option			Dim C	Dim D Dim N		Dim W1	Dim W2	Dim W3 (LSL-USL)		
12mm	7" Dia	7.00 177.8	0.059 1.5	512+0.020/-0.008 13+0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4		
12mm	13" Dia	13.00 330	0.059 1.5	512+0.020/-0.008 13+0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4		

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.