MT4410

N-Channel PowerTrench®MOSFET
30V, 18A, 4.5mΩ

MT Semiconductor®

http://www.mtsemi.com

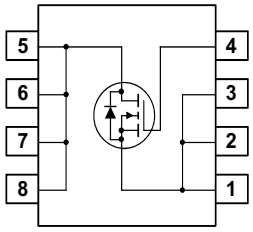
General Description

This N-Channel MOSFET has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.It has been optimized for low gate charge, low $R_{DS(on)}$ and fast switching speed.

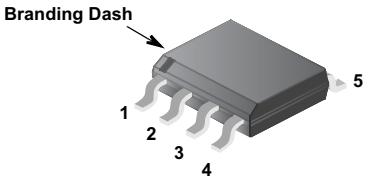
Features

- $R_{DS(on)}$ = 4.5mΩ , V_{GS} = 10V, I_D = 18A
- $R_{DS(on)}$ = 6.5mΩ , V_{GS} = 4.5V, I_D = 17A
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- RoHS compliant

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



SO-8

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 50°C/W)	18	A
	Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 50°C/W)	17	A
	Pulsed	134	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	420	mJ
P_D	Power dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	125	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT4410	MT4410	SO-8	330mm	12mm	2500 units

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT4410	MT4410	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V	-	-	1	μA
		V_{GS} = 0V, T_J = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2	-	2.5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 18A, V_{GS} = 10V	-	4.5	6.0	mΩ
		I_D = 17A, V_{GS} = 4.5V	-	6.5	9.0	
		I_D = 18A, V_{GS} = 10V, T_J = 150°C	-	5.5	7.2	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	1615	-	pF
C_{OSS}	Output Capacitance		-	500	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	150	-	pF
R_G	Gate Resistance	V_{GS} = 0.5V, f = 1MHz	0.5	2.0	3.5	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	85	112	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V; V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	45	62	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V; V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	4.6	6.0	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	11	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	6.4	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15V, I_D = 18A, I_g = 1.0mA	-	15	-	nC
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 18A, V_{GS} = 10V, R_{GS} = 3.3Ω	-	-	8.6	ns
$t_{d(ON)}$	Turn-On Delay Time		-	9	-	ns
t_r	Rise Time		-	8.4	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	16	-	ns
t_f	Fall Time		-	21	-	ns
t_{OFF}	Turn-Off Time		-	-	12.2	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 18A	-	-	1.25	V
		I_{SD} = 2.1A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 18A, dI_{SD}/dt = 100A/μs	-	-	37	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 18A, dI_{SD}/dt = 100A/μs	-	-	22	nC

Notes:

1: Starting T_J = 25°C, L = 1mH, I_{AS} = 29A, V_{DD} = 30V, V_{GS} = 10V.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.

a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad.

Typical Characteristics T_J = 25°C unless otherwise noted

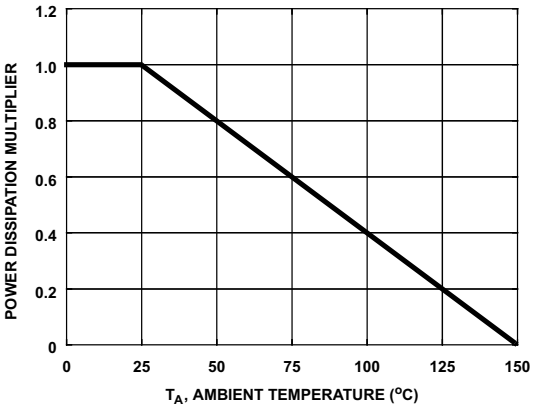


Figure 1. Normalized Power Dissipation vs Ambient Temperature

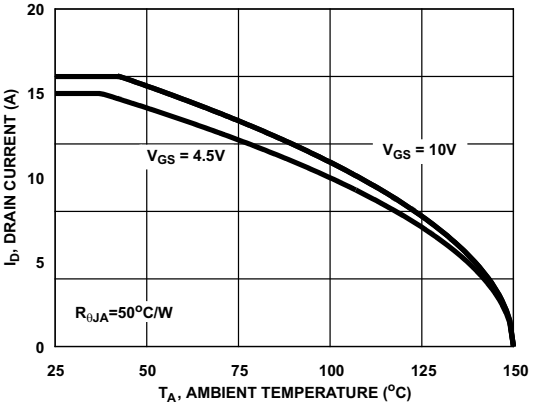


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

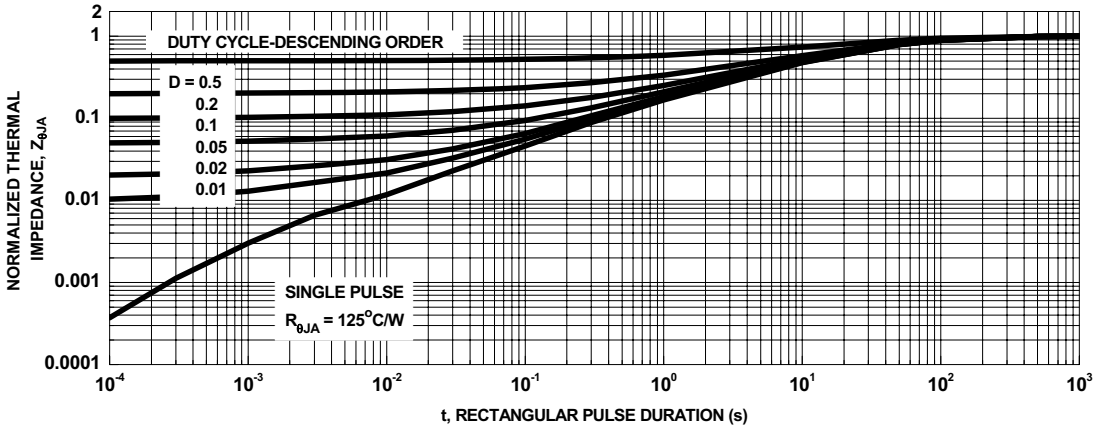


Figure 3. Normalized Maximum Transient Thermal Impedance

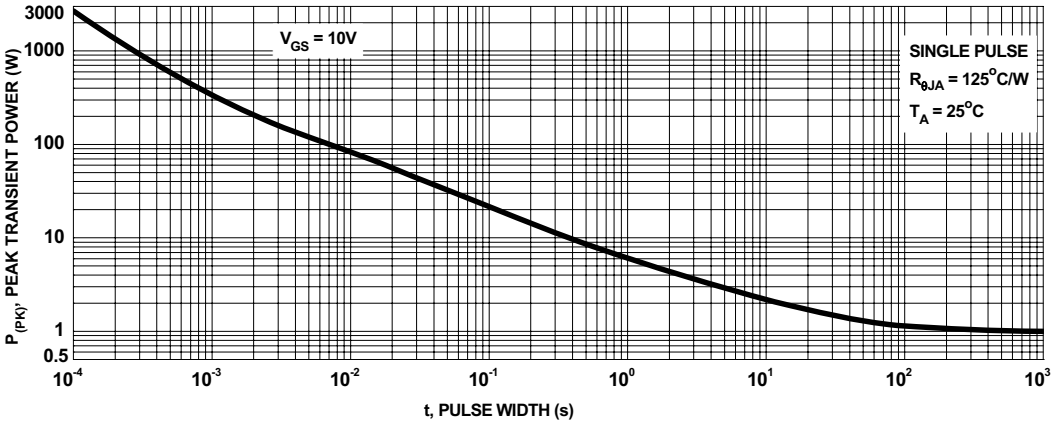
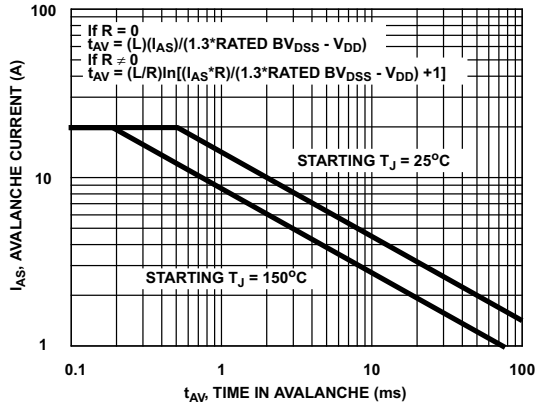


Figure 4. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching Capability

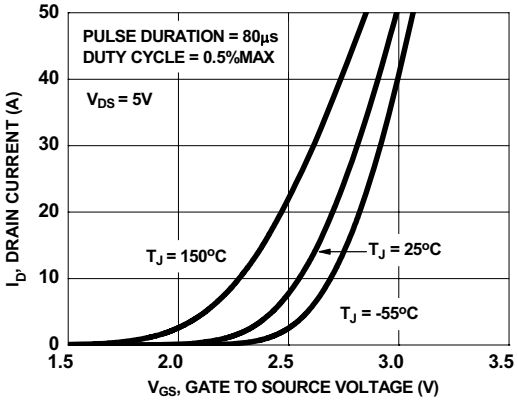


Figure 6. Transfer Characteristics

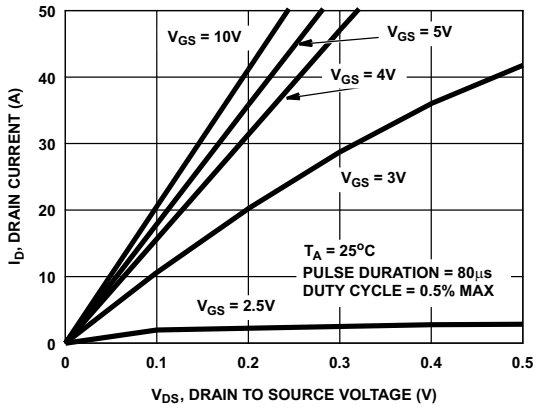


Figure 7. Saturation Characteristics

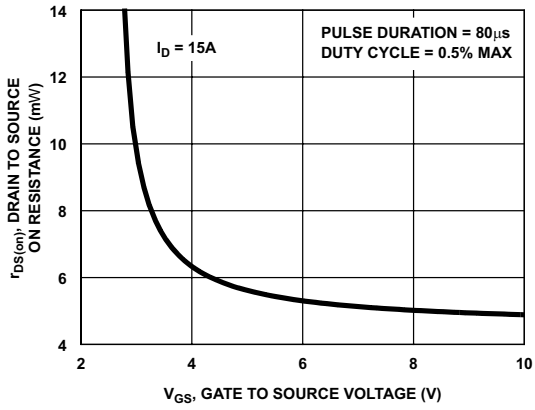


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

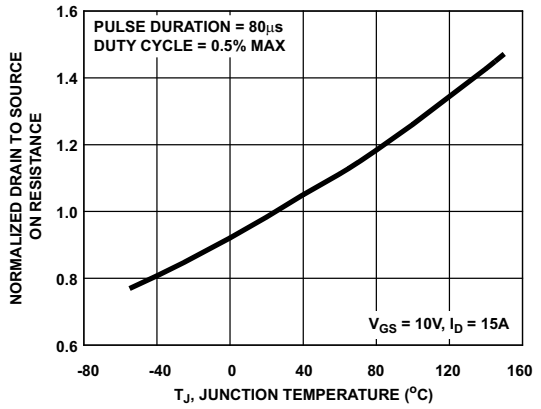


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

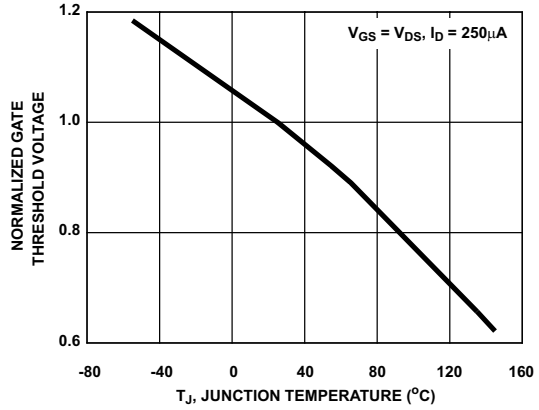


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

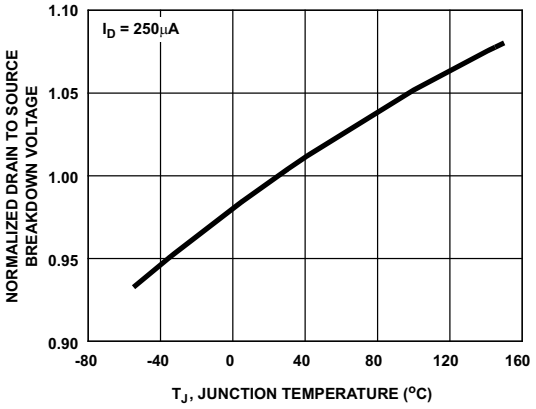


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

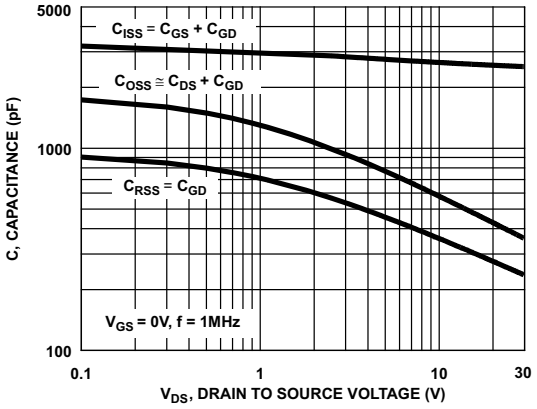


Figure 12. Capacitance vs Drain to Source Voltage

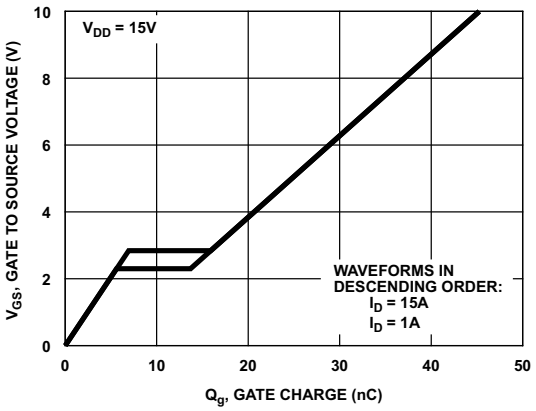


Figure 13. Gate Charge Waveforms for Constant Gate Currents

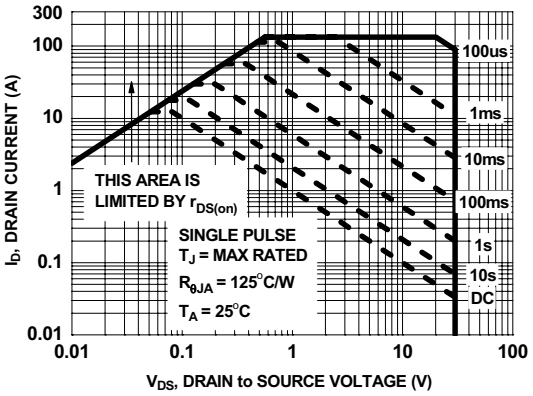


Figure 14. Forward Bias Safe Operating Area

Test Circuits and Waveforms

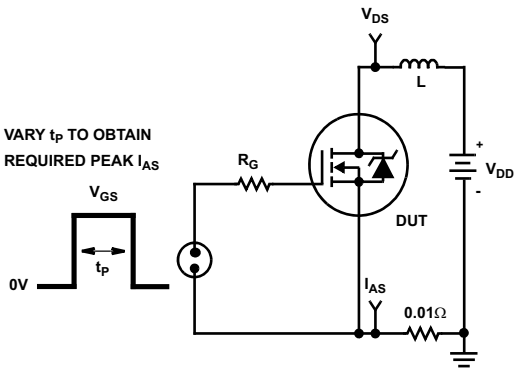


Figure 15. Unclamped Energy Test Circuit

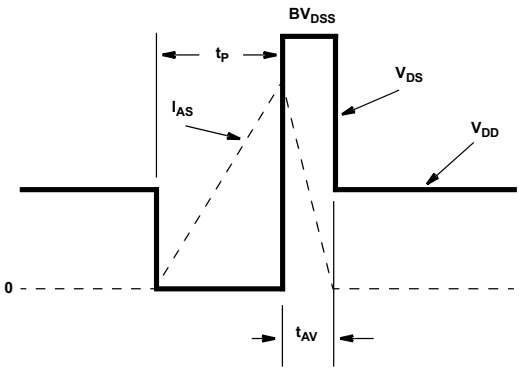


Figure 16. Unclamped Energy Waveforms

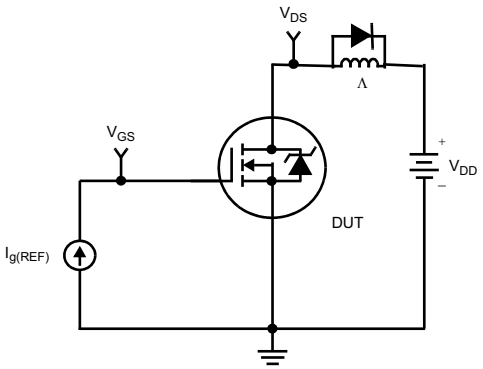


Figure 17. Gate Charge Test Circuit

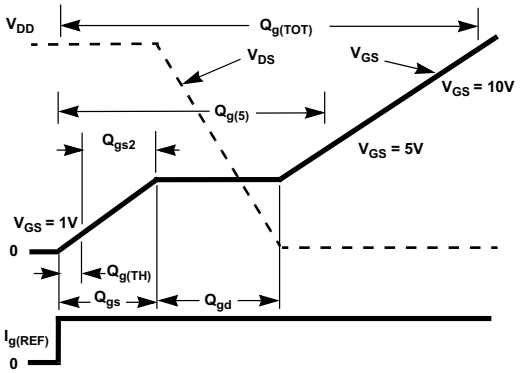


Figure 18. Gate Charge Waveforms

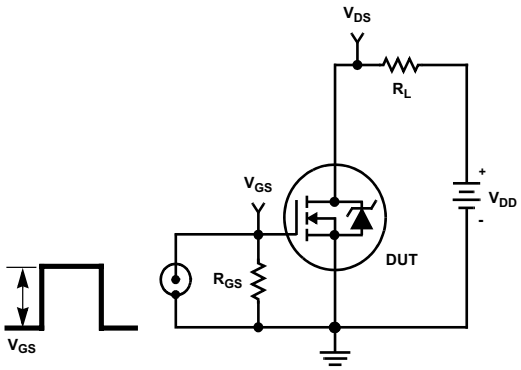


Figure 19. Switching Time Test Circuit

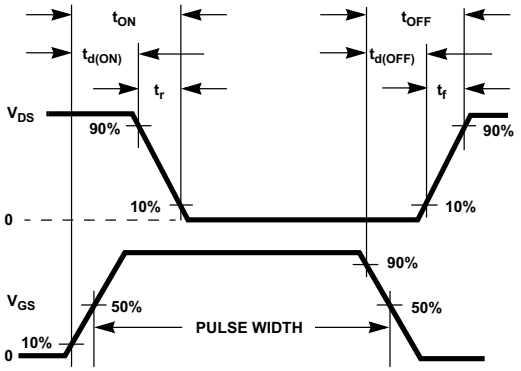


Figure 20. Switching Time Waveforms

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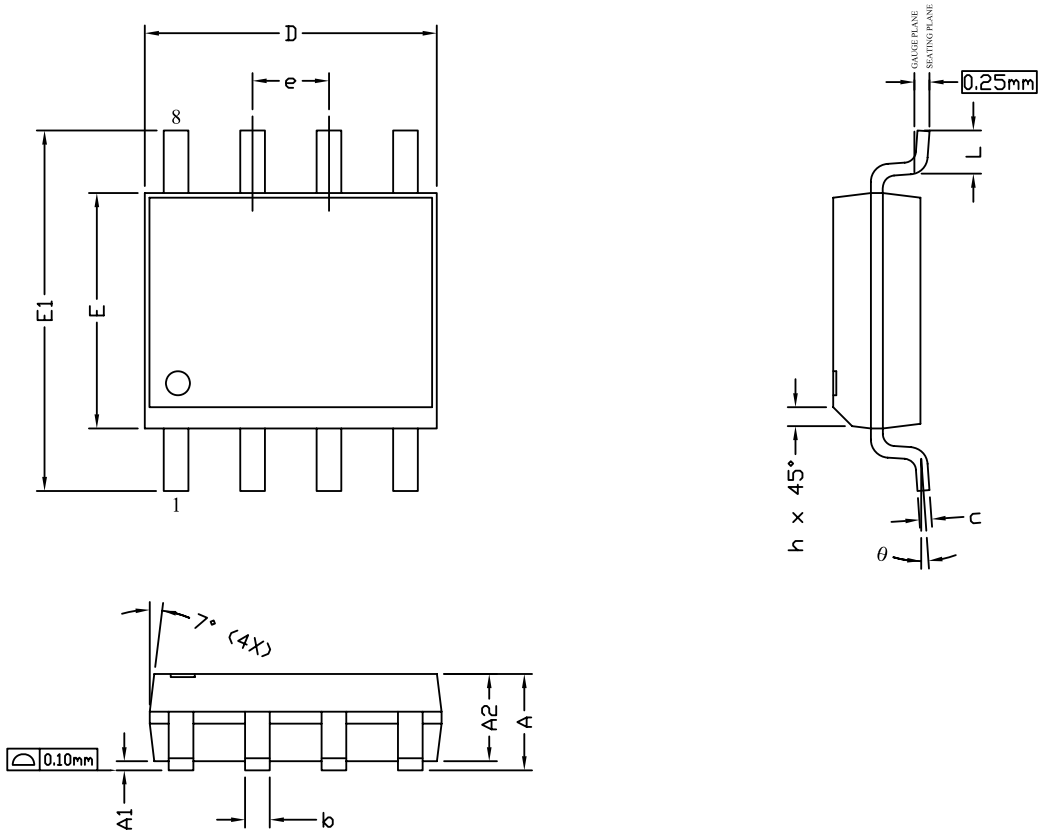
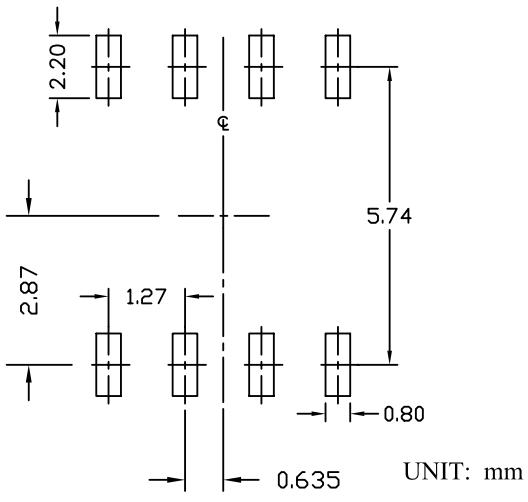
SO8 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	----	0.51	0.012	----	0.020
c	0.17	----	0.25	0.007	----	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	----	0.50	0.010	----	0.020
L	0.40	----	1.27	0.016	----	0.050
θ	0°	----	8°	0°	----	8°

NOTE
1. ALL DIMENSIONS ARE IN MILLMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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8. 除上述第7项内容外，不能将本资料中记载的产品用于以下用途。如果用于以下用途而造成的损失，本公司概不负责。
   1）生命维持装置。
   2）植埋于人体使用的装置。
   3）用于治疗（切除患部、给药等）的装置。
   4）其他直接影响到人的生命的装置。
9. 在使用本资料所记载的产品时，对于最大额定值、工作电源电压的范围、放热特性、安装条件及其他条件请在本公司规定的保证范围内使用。如果超出了本公司规定的保证范围使用时，对于由此而造成的故障和出现的事故，本公司将不承担任何责任。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.