

MT4605

20V Complementary Power MOSFET

Features

- N-Channel
20V/5.6A
 $R_{DS(ON)} = 19m\Omega$ (Typ.) @ $V_{GS} = 4.5V$
 $R_{DS(ON)} = 23m\Omega$ (Typ.) @ $V_{GS} = 2.5V$
- P-Channel
-20V/-4.5A
 $R_{DS(ON)} = 75m\Omega$ (Typ.) @ $V_{GS} = -4.5V$
 $R_{DS(ON)} = 110m\Omega$ (Typ.) @ $V_{GS} = -2.5V$
- RoHS Compliant

General Description

This complementary MOSFET device is produced using Mos-tech's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC-DC converter
- Power management
- LCD backlight inverter

Absolute Maximum Ratings

$T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-CH	P-CH	Units
V _{DSS}	Drain-Source Voltage	20	-20	V
V _{GSS}	Gate-Source Voltage	±12	±12	V
I _D	Drain Current - Continuous			

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	15	$^\circ C/W$

Package Marking and Ordering Information

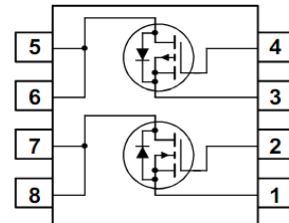
Device Marking	Device	Reel Size	Tape width	Quantity
MT4605	MT4605	13"	12mm	2500 units



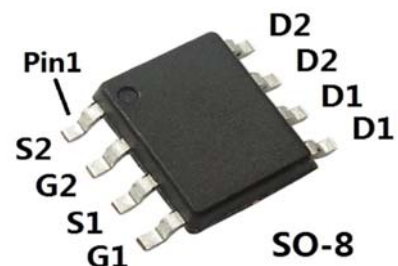
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	N-CH P-CH	20 -20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	N-CH P-CH	-	21 -13	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	N-CH P-CH	-	-	1 -1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$	N-CH P-CH	-	-	± 100 ± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	N-CH P-CH	0.5 -0.5	0.7 -0.7	1.2 -1.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	N-CH P-CH	-	-3.6 2.5	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{ V}, I_D=5.0\text{ A}$ $V_{GS}=2.5\text{ V}, I_D=3.5\text{ A}$	N-CH	- -	19 23	23 28	m Ω
		$V_{GS}=-4.5\text{ V}, I_D=-4.0\text{ A}$ $V_{GS}=-2.5\text{ V}, I_D=-3.0\text{ A}$	P-CH	- -	75 110	80 120	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	N-CH P-CH	5.6 -4.5	-	-	A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 4.5\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$	N-CH P-CH	-	15 12	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	N-CH $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-CH P-CH	-	515 6	-	pF
C_{oss}	Output Capacitance	P-CH	N-CH P-CH	-	90 6	-	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-CH P-CH	-	72 6	-	pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	N-CH $V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 1\text{ }\Omega$	N-CH P-CH	-	3 5	-	ns
t_r	Turn-On Rise Time		N-CH P-CH	-	7.5 12	-	ns
$t_{d(off)}$	Turn-Off Delay Time	P-CH $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 1\text{ }\Omega$	N-CH P-CH	-	20 25	-	ns
t_f	Turn-Off Fall Time		N-CH P-CH	-	6 10	-	ns
Q_g	Total Gate Charge	N-CH $V_{DS} = 10\text{ V}, I_D = 4.5\text{ A}, V_{GS} = 10\text{ V}$	N-CH P-CH	-	12 10	-	nC
Q_{gs}	Gate-Source Charge	P-CH	N-CH P-CH	-	1 0.8	-	nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = -10\text{ V}, I_D = -3.5\text{ A}, V_{GS} = -10\text{ V}$	N-CH P-CH	-	2 1.8	-	nC

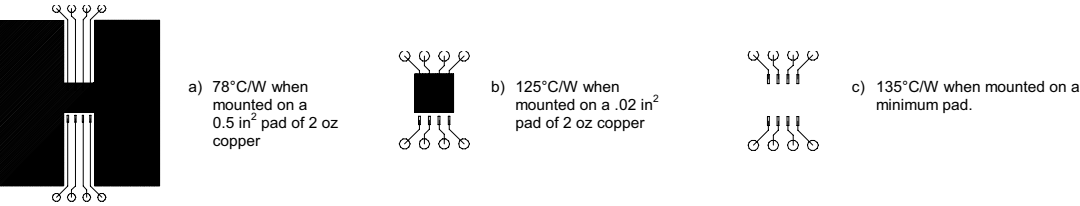
Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Diode Characteristics and Maximum Ratings

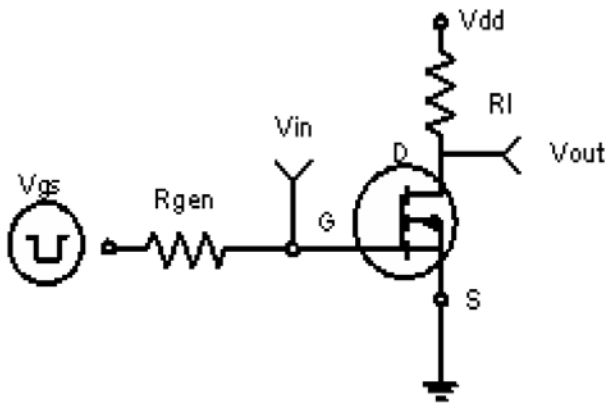
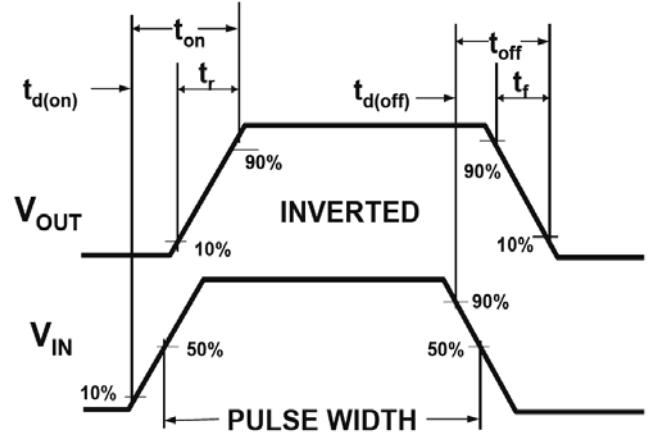
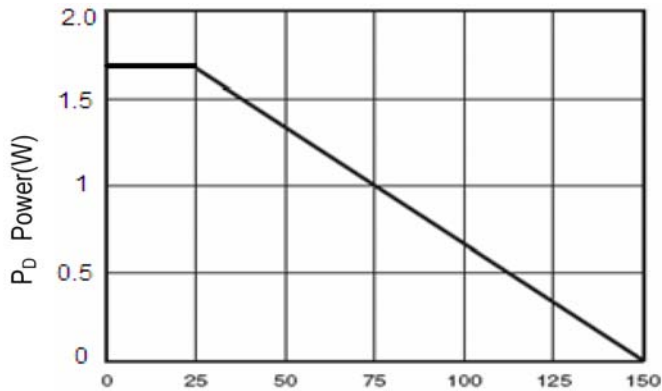
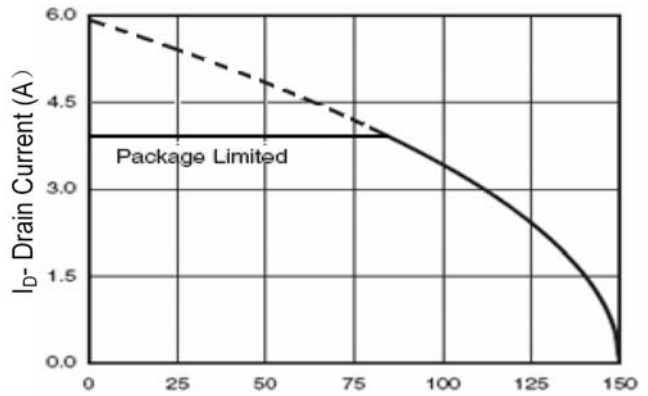
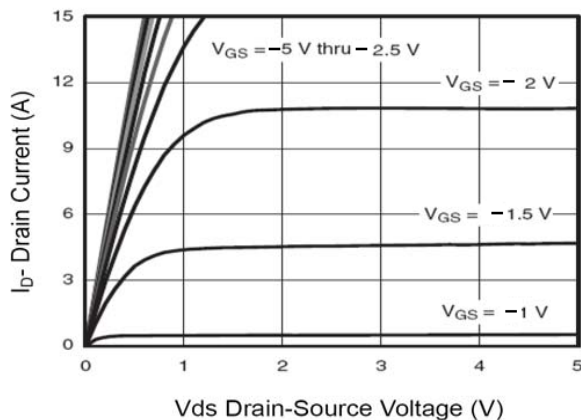
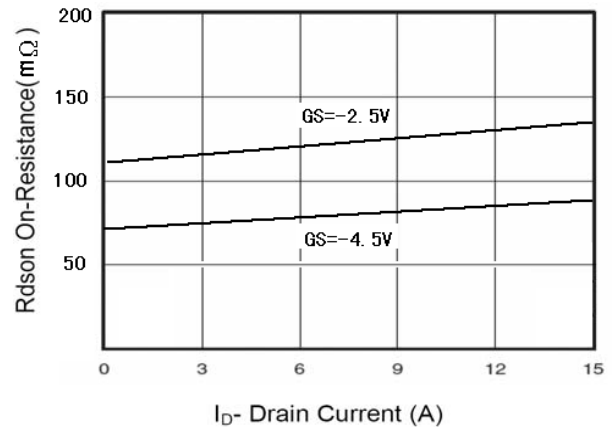
I _S	Maximum Continuous Drain-Source Diode Forward Current		N-CH P-CH	-	-	1.4 -1.4	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1 A (Note 2) V _{GS} = 0 V, I _S = -3.5 A (Note 2)	N-CH P-CH	-	1.3 -1.2	-	V

Notes:
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS P-CH**Typical Electrical and Thermal Characteristics****Figure 1: Switching Test Circuit****Figure 2: Switching Waveforms****Figure 3 Power Dissipation****Figure 4 Drain Current****Figure 5 Output Characteristics****Figure 6 Drain-Source On-Resistance**

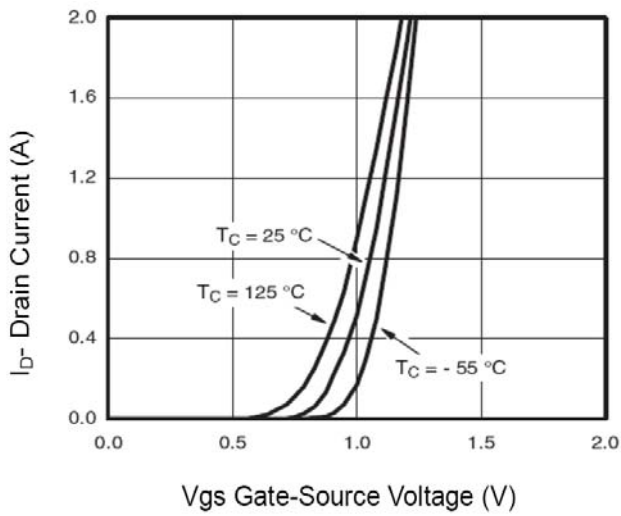


Figure 7 Transfer Characteristics

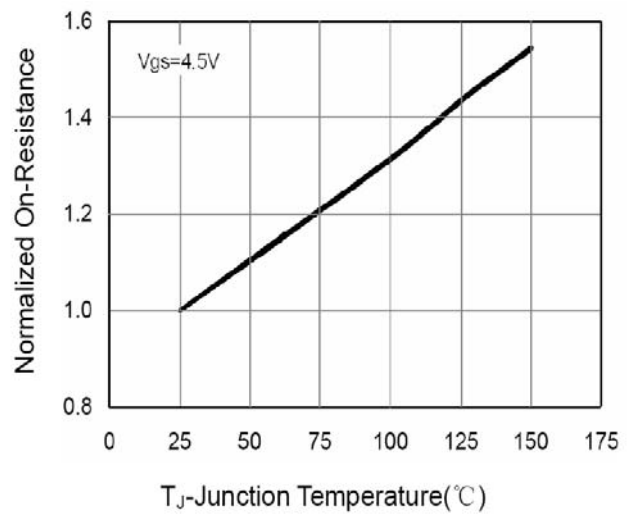


Figure 8 Drain-Source On-Resistance

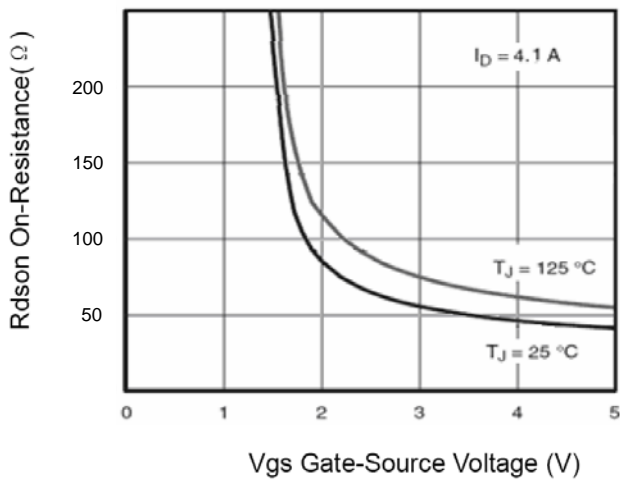


Figure 9 Rdson vs Vgs

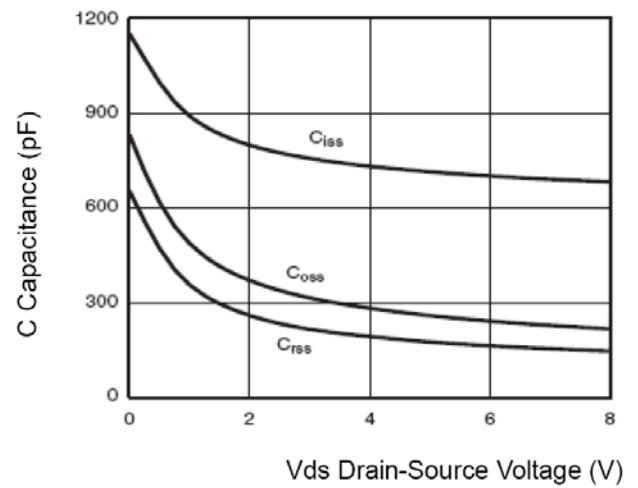


Figure 10 Capacitance vs Vds

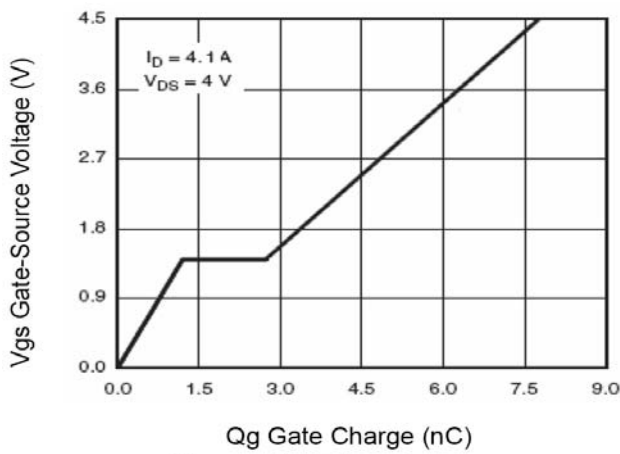


Figure 11 Gate Charge

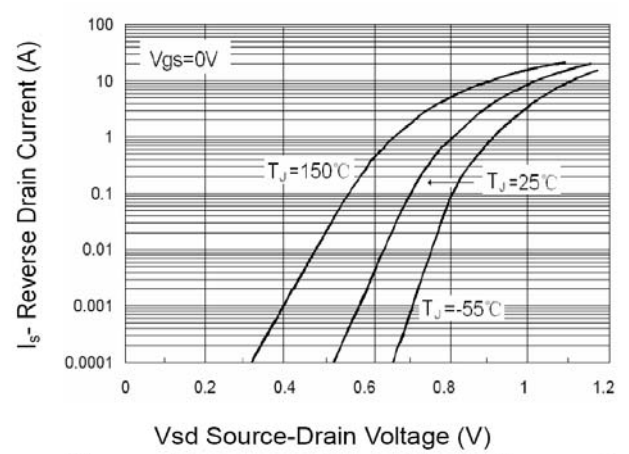


Figure 12 Source- Drain Diode Forward

Typical Characteristics: N-CH

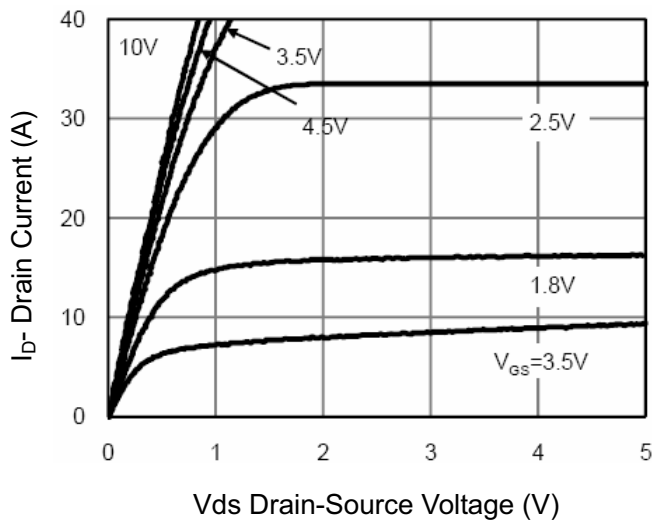


Figure 1 Output Characteristics

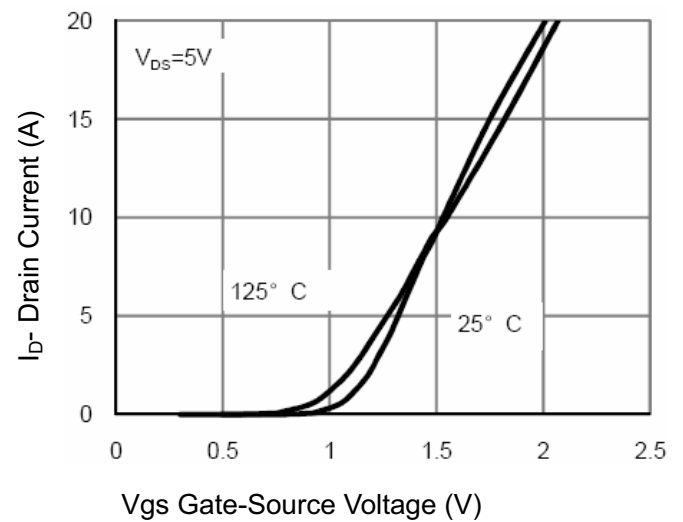


Figure 2 Transfer Characteristics

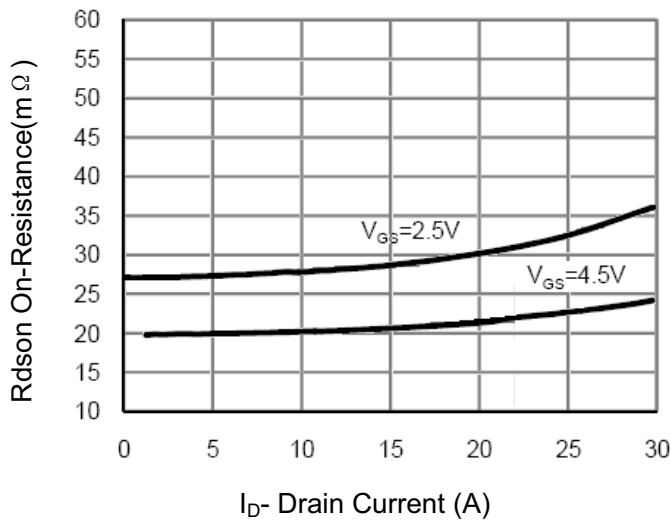


Figure 3 Drain-Source On-Resistance

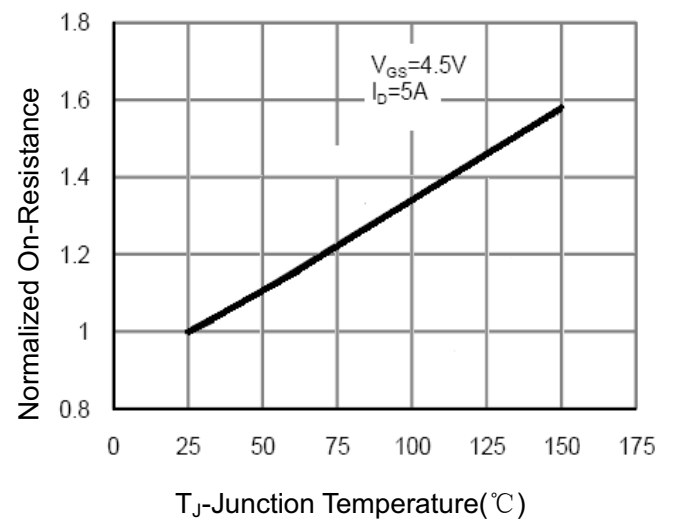


Figure 4 Drain-Source On-Resistance

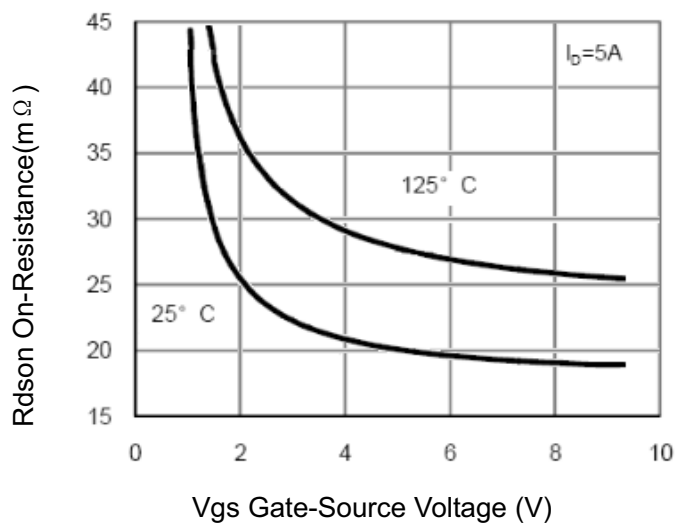
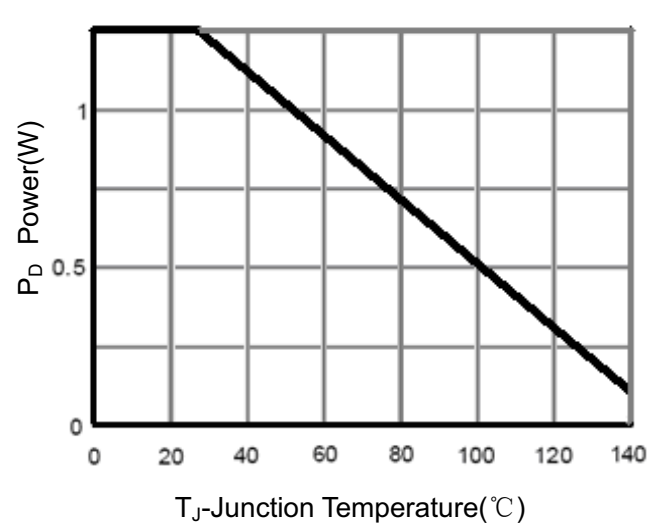


Figure 5 Rdson vs Vgs



Typical Characteristics: N-CH

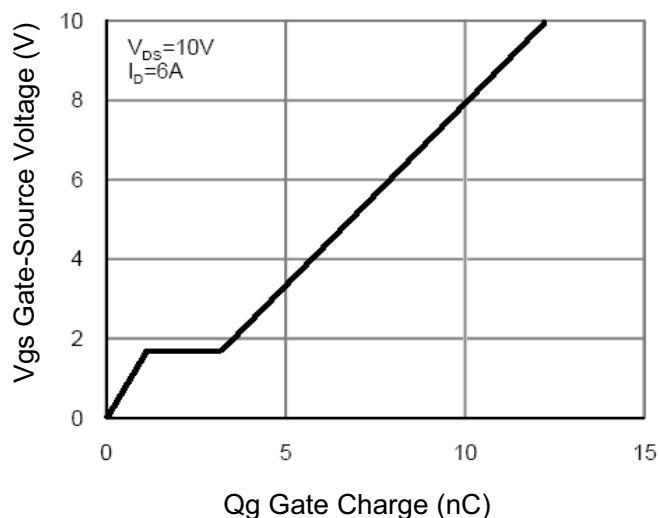


Figure 7 Gate Charge

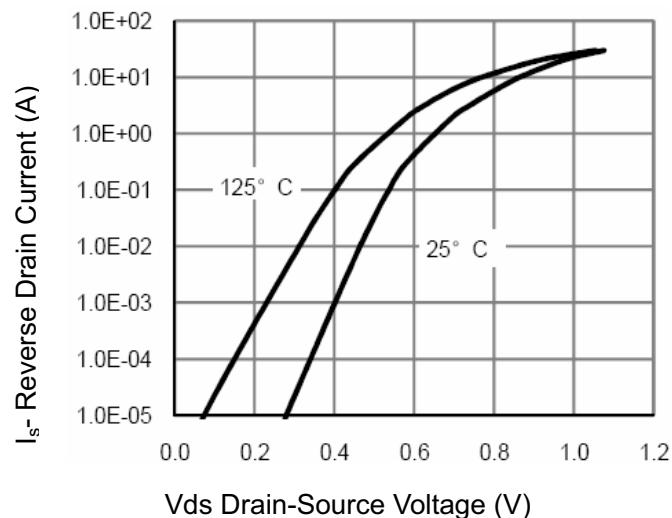


Figure 8 Source- Drain Diode Forward

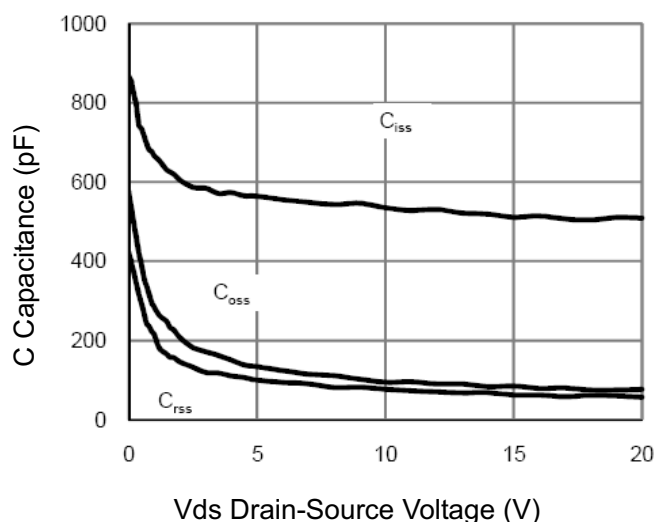


Figure 9 Capacitance vs Vds

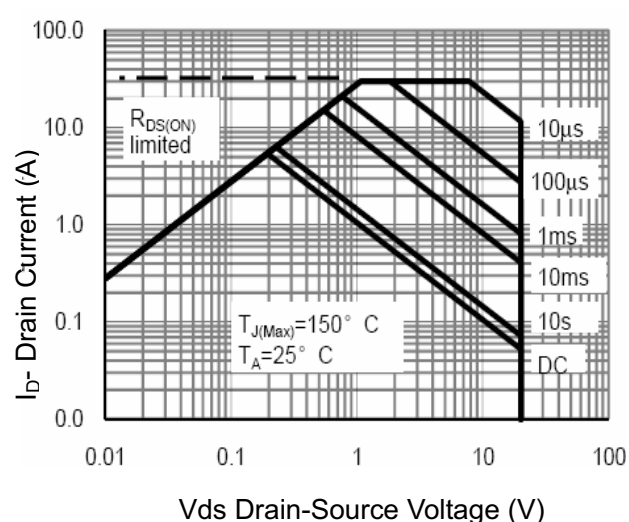


Figure 10 Safe Operation Area

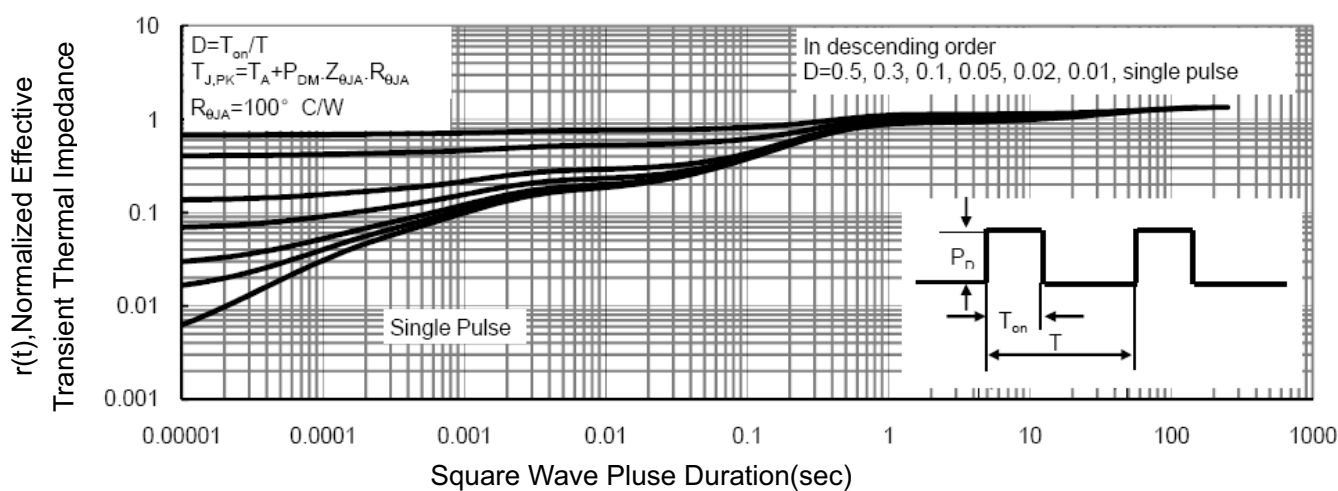


Figure 11 Normalized Maximum Transient Thermal Impedance

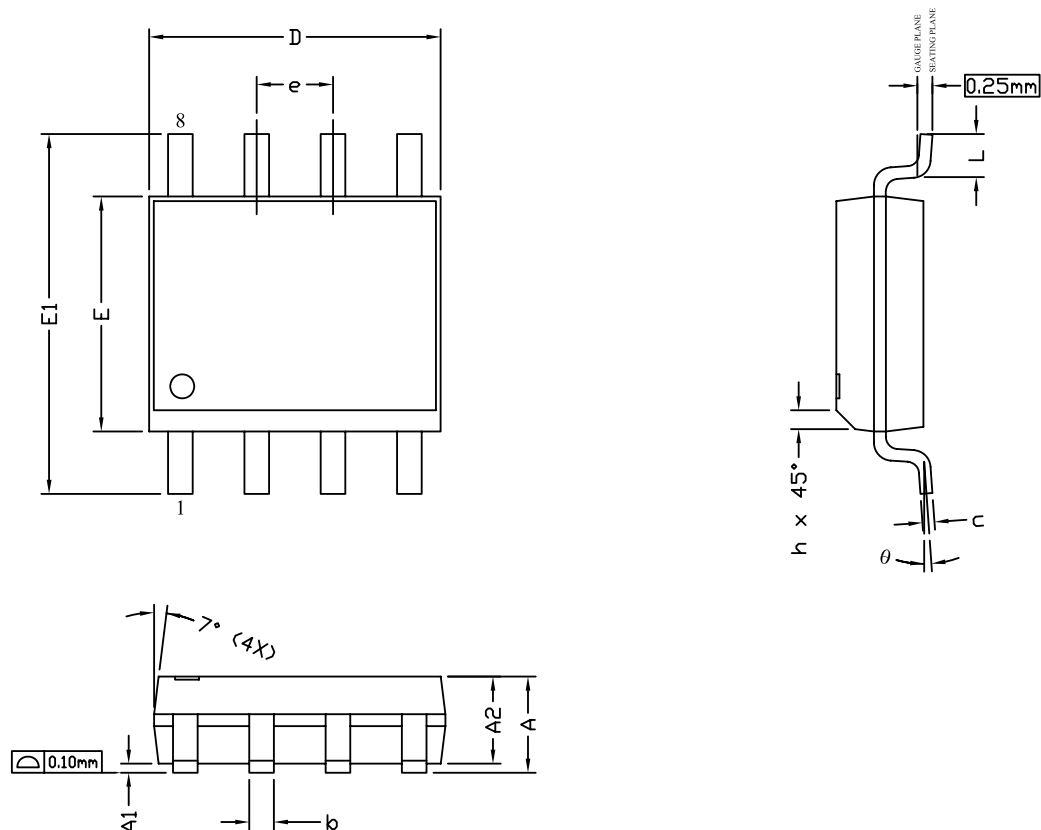
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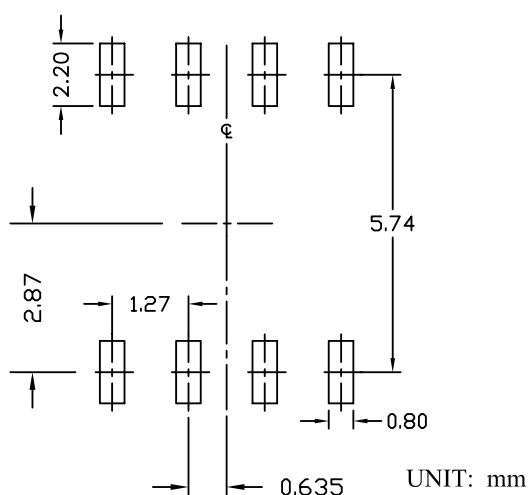
Version

rev H

S08 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
θ	0°	—	8°	0°	—	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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10. 本公司一直致力于提高产品的质量和可靠性, 但一般来说, 半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失, 希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等, 这是作为机器和系统的出厂保证。特别是单片机的软件, 由于单独进行验证很困难, 所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
11. 如果把本资料所记载的产品从其载体设备上卸下, 有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时, 请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时, 本公司将不承担任何责任。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.