

MT4953A

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = -20V$
- $I_D = -5A$
- $R_{DS(ON)} 60m\Omega$
@ $V_{GS} = -10V/-4.9A$
- $R_{DS(ON)} 75m\Omega$
@ $V_{GS} = -4.5V/-3.6A$

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

Applications :

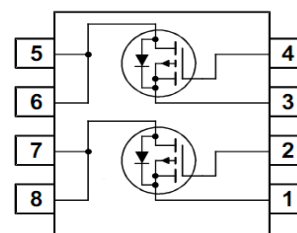
- Load Switch.
- PWM Applications.



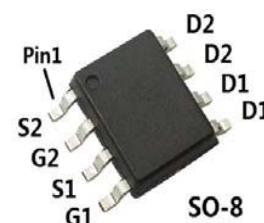
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Steady State	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current ¹	-5	A
I_{DM}	Pulsed Drain Current ²	-27	A
I_S	Continuous Source Current (Diode Conduction) ¹	-2	A
P_D	Maximum Power Dissipation ¹	1.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55~150	$^\circ C$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board, $t \leq 10$ Sec.
2. Pulse width limited by maximum junction temperature.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT4953A	MT4953A	SO-8	-	-	2500

Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
R _{thJA}	Maximum Junction-to-Ambient	t ≤ 10 Sec	45	69	°C/W
		Steady State	85	104	
R _{thJF}	Maximum Junction-to-Foot (Drain)	Steady State	37	46	

Electrical Characteristics (T_A=25°C, unless otherwise noted)

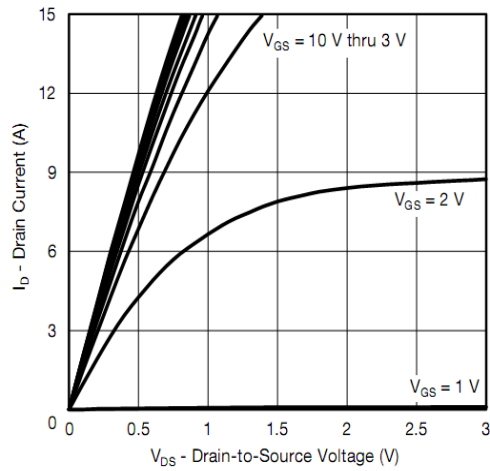
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
• Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-20	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.7	-1.1	-1.2	V
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	-	-	-1	μA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 85°C	-	-	-30	
R _{DS(on)}	Drain Source On State Resistance ^a	V _{GS} = -10V, I _D = -4.9A	-	60	65	mΩ
		V _{GS} = -4.5V, I _D = -3.6A	-	75	84	
g _{fs}	Forward Transconductance ^a	V _{DS} = -5V, I _D = -4A	-	16	-	S
V _{SD}	Diode Forward Voltage ^a	V _{GS} = 0V, I _S = -1A	-	-0.8	-1.2	V
• Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1MHz	-	1360	-	pF
C _{oss}	Output Capacitance		-	240	-	
C _{rss}	Reverse Transfer Capacitance		-	170	-	
Q _g	Total Gate Charge	V _{DS} = -15V, V _{GS} = -4.5V, I _D = -5A	-	14	-	nC
Q _{gs}	Gate-Source Charge		-	2.6	-	
Q _{gd}	Gate-Drain Charge		-	5.2	-	
t _{d(on)}	Turn-On Delay Time	V _{DD} = -15V, R _L = 3Ω I _D = -1.0A, V _{GEN} = -10V, R _G = 6Ω	-	17	-	nSec
t _r	Rise Time		-	14	-	
T _{d(off)}	Turn-Off Delay Time		-	65	-	
t _f	Fall Time		-	29	-	
R _g	Gate Resistance	V _{GS} = 0, V _{DS} = 0, f = 1MHz	-	8	-	Ω
t _{rr}	Body Diode Reverse Recovery Time	I _F = -4A, di/dt = 100A/μs	-	25	-	nSec
Q _{rr}	Body Diode Reverse Recovery Charge		-	10	-	nC

Note:

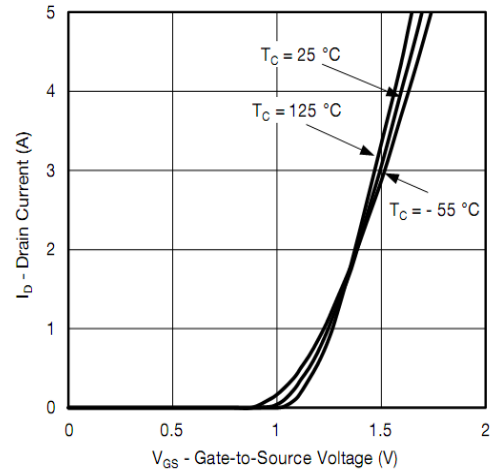
a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

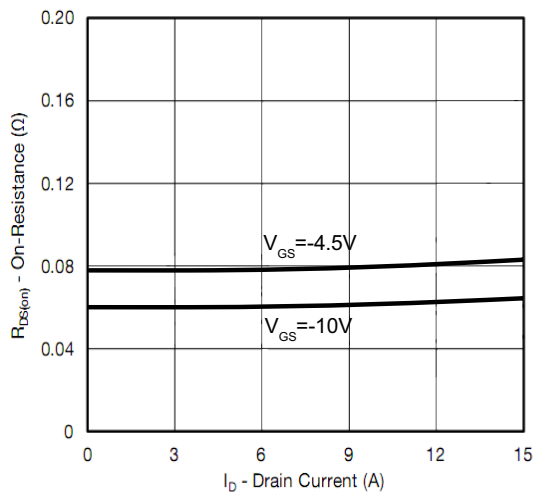
Characteristics Curve



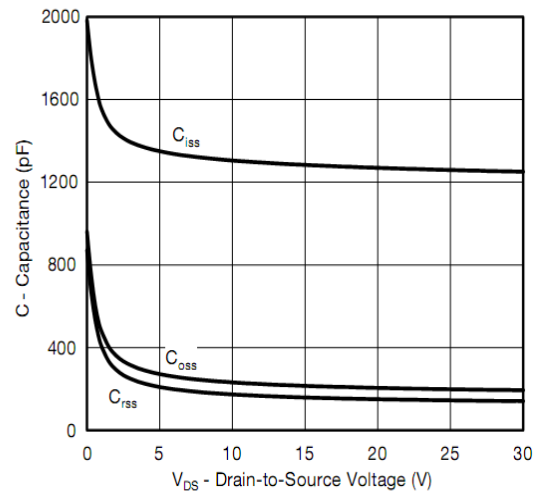
Output Characteristics



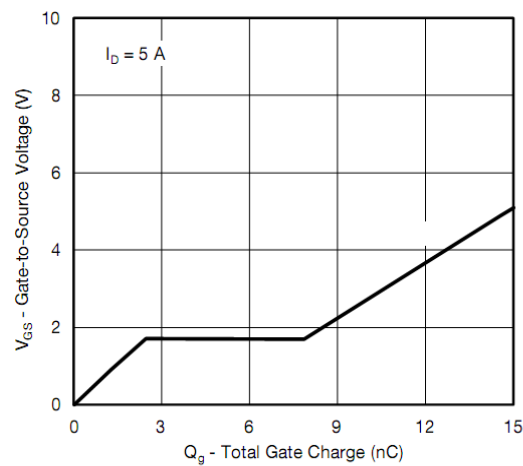
Transfer Characteristics



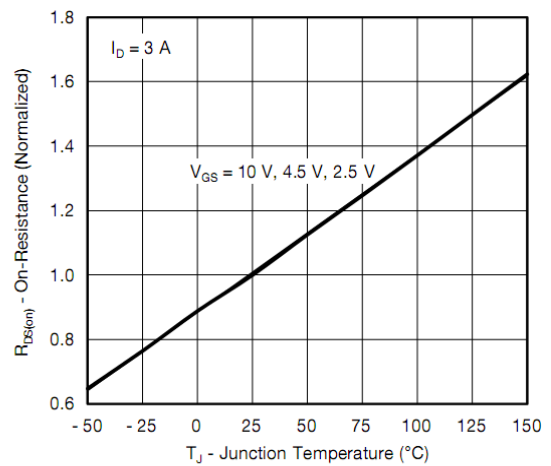
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

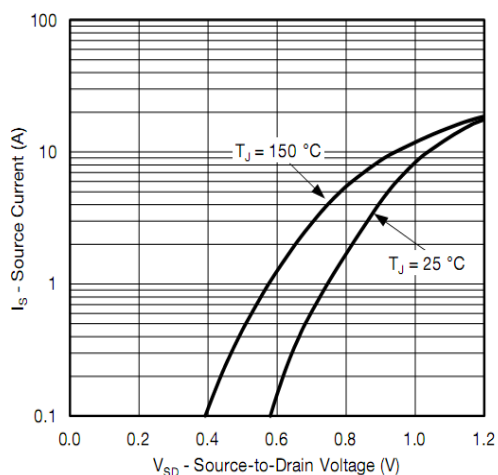


Gate Charge

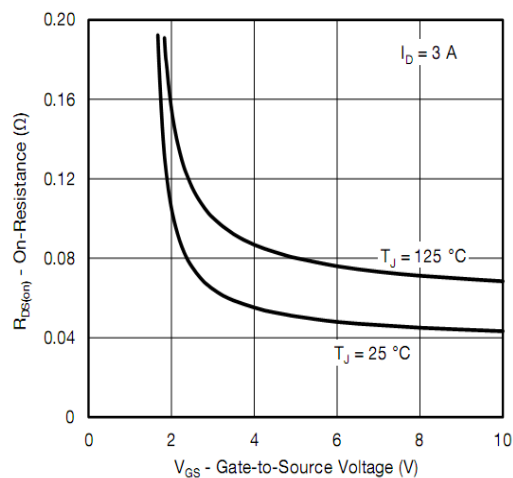


On-Resistance vs. Junction Temperature

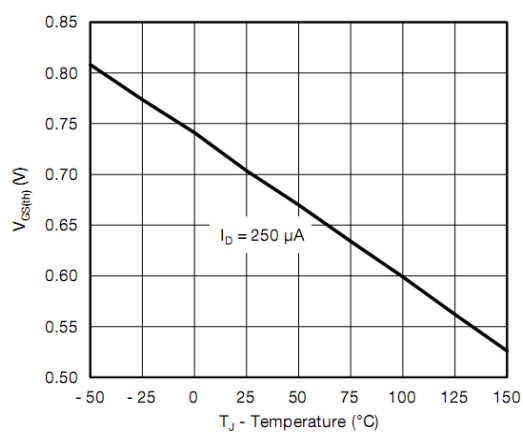
Characteristics Curve



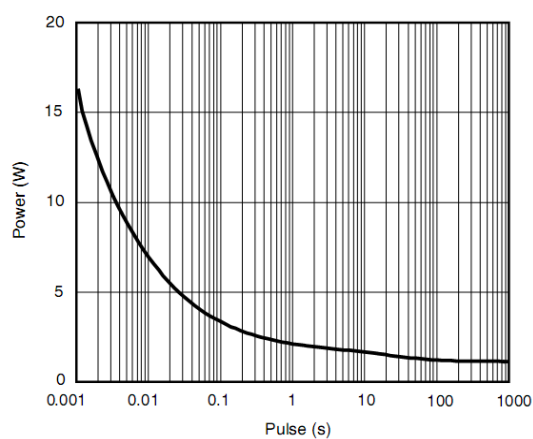
Source-Drain Diode Forward Voltage



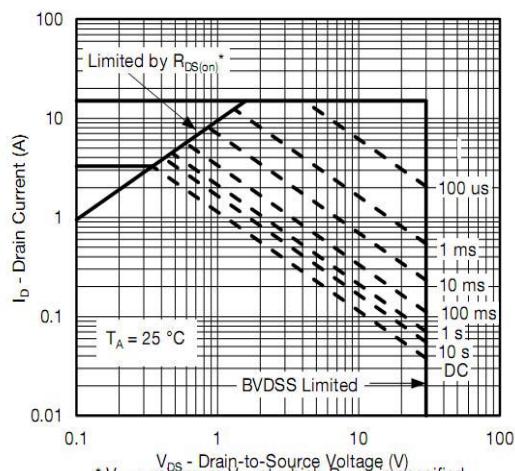
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

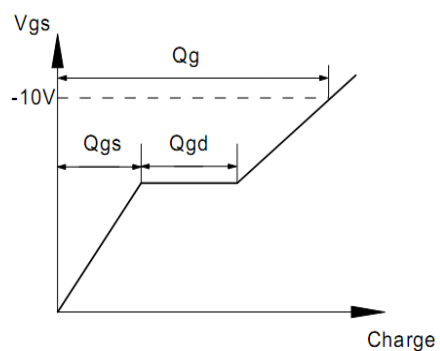
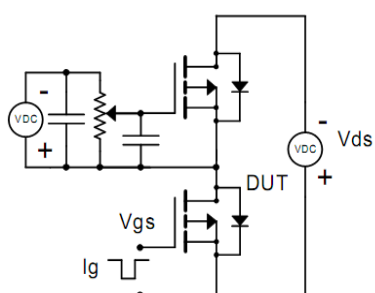


Single Pulse Power, Junction-to-Ambient



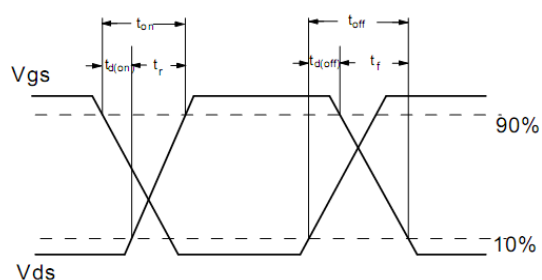
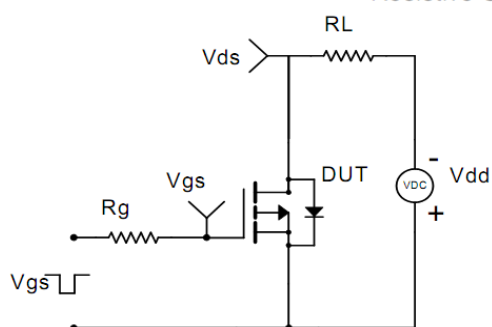
Safe Operating Area, Junction-to-Ambient

Gate Charge Test Circuit & Waveform

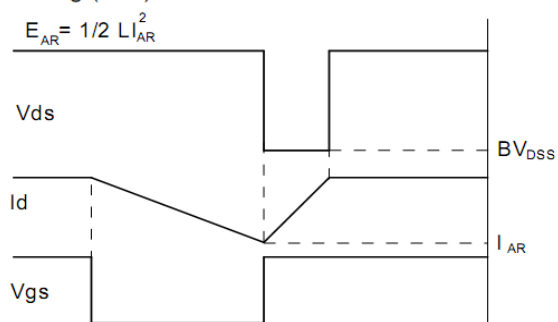
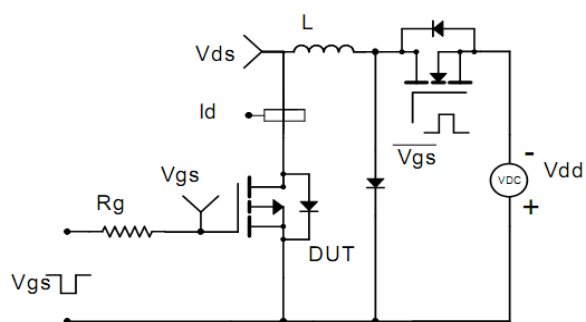


Resistive Switching Test Circuit & Waveforms

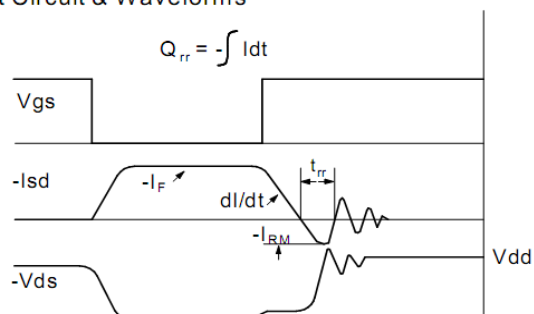
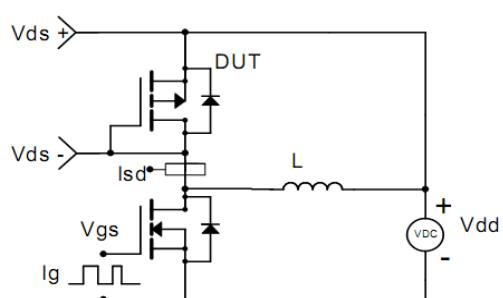
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

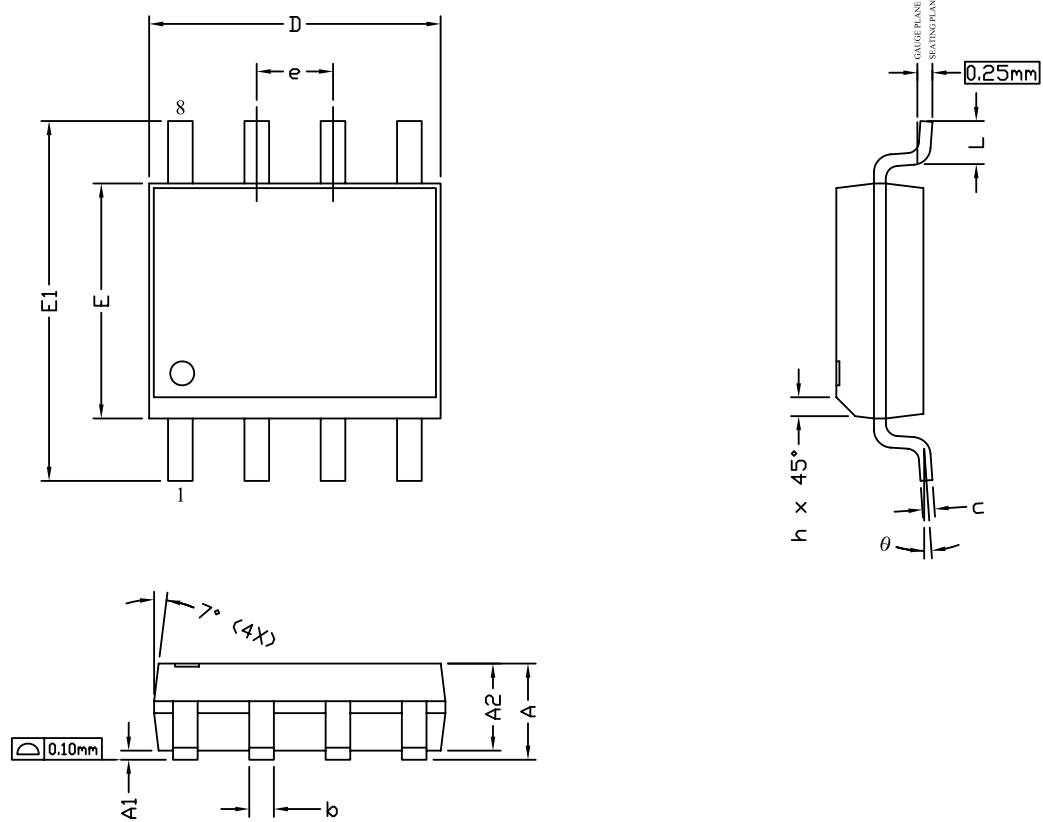


Diode Recovery Test Circuit & Waveforms

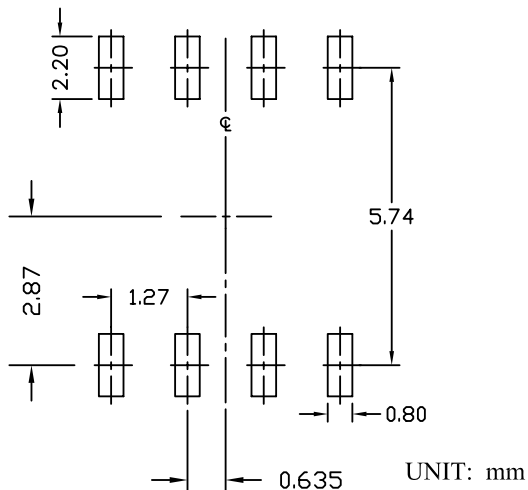


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Version	rev H

S08 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
θ	0°	—	8°	0°	—	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Part Marking Information

SO-8 (PMG Code)

SO-8 Devices



MT4953A = Example Base Part Number

● = Pin 1 Indicator

△ = ESD Symbol (⚡)

9 = Year Code

A = Month Code

3 = Week Code

H = Assembly Factory Code

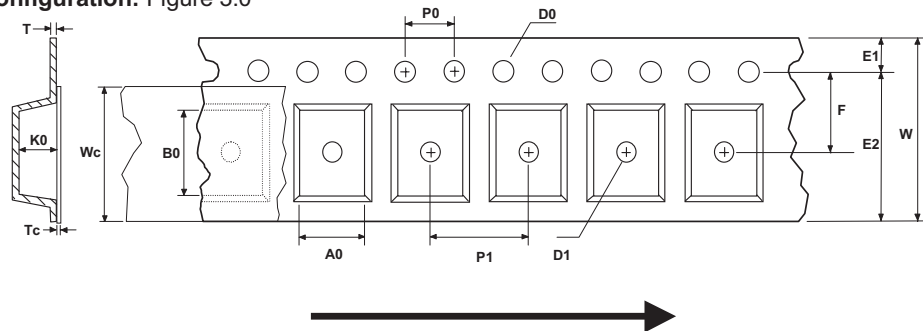
NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

SO-8 Tape and Reel Data, continued

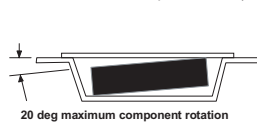
SO(8lds) Embossed Carrier Tape Configuration: Figure 3.0



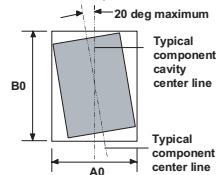
Dimensions are in millimeter

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

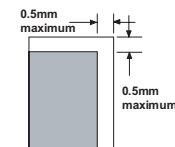
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

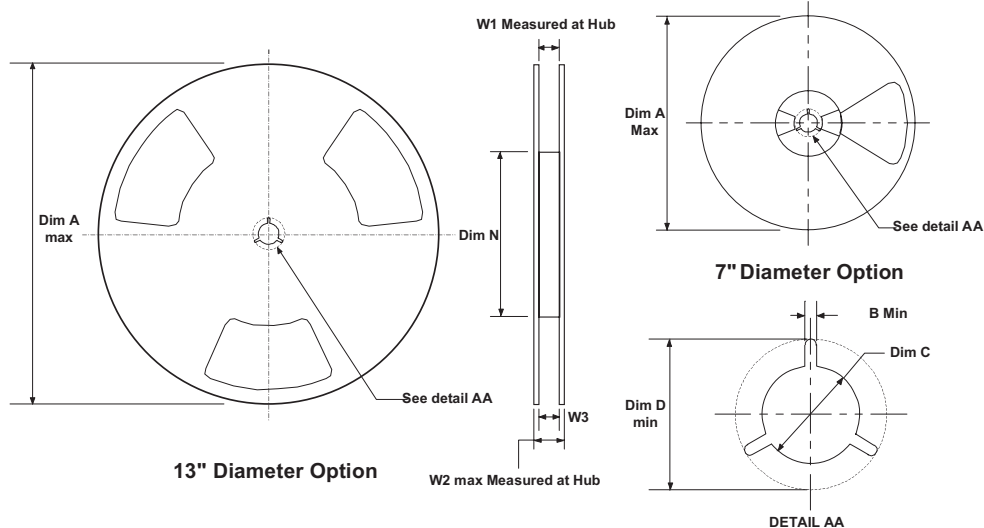


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512+0.020/-0.008 13+0.5/-0.2	0.795 20.2	2.165 55	0.488+0.078/-0.000 12.4+2/0	0.724 18.4	0.469-0.606 11.9-15.4
12mm	13" Dia	13.00 330	0.059 1.5	512+0.020/-0.008 13+0.5/-0.2	0.795 20.2	7.00 178	0.488+0.078/-0.000 12.4+2/0	0.724 18.4	0.469-0.606 11.9-15.4

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.