

MT4976

60V Complementary Power MOSFET

Features

- N-Channel
60V/4.5A,
 $R_{DS(ON)} = 40m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} = 45m\Omega @ V_{GS} = 4.5V$
- P-Channel
-60V/-3.5A,
 $R_{DS(ON)} = 75m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} = 90m\Omega @ V_{GS} = -4.5V$
- RoHS Compliant

General Description

This complementary MOSFET device is produced using Mos-tech's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC-DC converter
- Power management
- LCD backlight inverter

Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-CH	P-CH	Units
V_{DSS}	Drain-Source Voltage	60	-60	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	4.5	-3.5	A
	- Pulsed	20	-20	
P_D	Power Dissipation for Dual Operation	2.3		W
	Power Dissipation for Single Operation (Note 1a)	1.8		
	(Note 1b)	1.4		
	(Note 1c)	2.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	79	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	41	$^\circ C/W$

Package Marking and Ordering Information

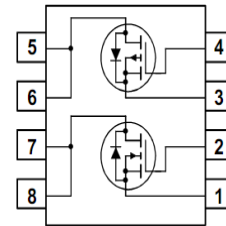
Device Marking	Device	Reel Size	Tape width	Quantity
MT4976	MT4976	13"	12mm	2500 units



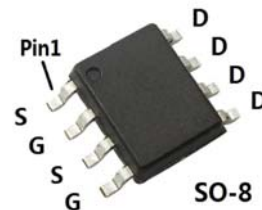
MT Semiconductor[®]

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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 1)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30\text{ V}, I_D = 4.5\text{ A}$	N-CH			93	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		N-CH			4.5	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	N-CH P-CH	60 -60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	N-CH P-CH		59 -47		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$	N-CH P-CH			1 -1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	N-CH P-CH			± 100 ± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	N-CH P-CH	1 -1	2.0 -2.0	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	N-CH P-CH		-5.6 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -3.5\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -3.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$	N-CH P-CH		40 52 45 75 95 90	50 64 55 100 130 120	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	N-CH P-CH	20 -20			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 4.5\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$	N-CH P-CH		15 10		S

Dynamic Characteristics

C_{iss}	Input Capacitance	N-CH $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-CH P-CH		853 980		pF
C_{oss}	Output Capacitance	P-CH	N-CH P-CH		60 48		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-CH P-CH		29 35		pF

Switching Characteristics (Note 2)

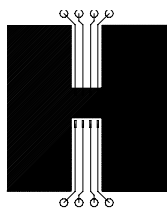
$t_{d(on)}$	Turn-On Delay Time	N-CH $V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	N-CH P-CH		6 9.7		ns
t_r	Turn-On Rise Time		N-CH P-CH		6 5.5		ns
$t_{d(off)}$	Turn-Off Delay Time	P-CH $V_{DD} = -30\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	N-CH P-CH		19 29		ns
t_f	Turn-Off Fall Time		N-CH P-CH		2.5 6		ns
Q_g	Total Gate Charge	N-CH $V_{DS} = 30\text{ V}, I_D = 4.5\text{ A}, V_{GS} = 10\text{ V}$	N-CH P-CH		20 23.7		nC
Q_{gs}	Gate-Source Charge	P-CH	N-CH P-CH		3 2.1		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = -30\text{ V}, I_D = -3.5\text{ A}, V_{GS} = -10\text{ V}$	N-CH P-CH		4.5 7.2		nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

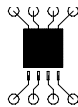
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-CH P-CH			1.4 -1.4	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	N-CH P-CH		0.8 -0.8	1.1 -1.1	V

Notes:

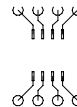
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics: P-CH

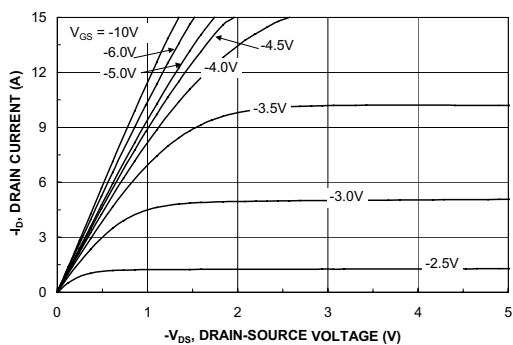


Figure 1. On-Region Characteristics.

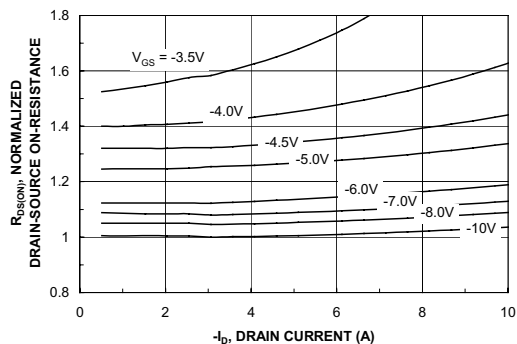


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

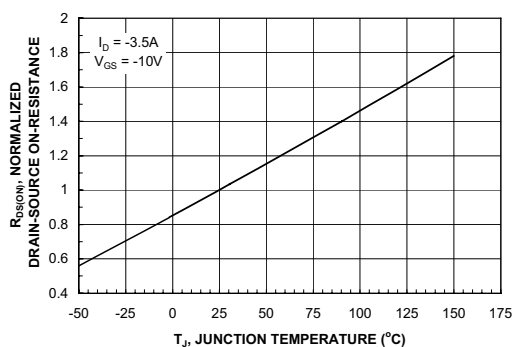


Figure 3. On-Resistance Variation with Temperature.

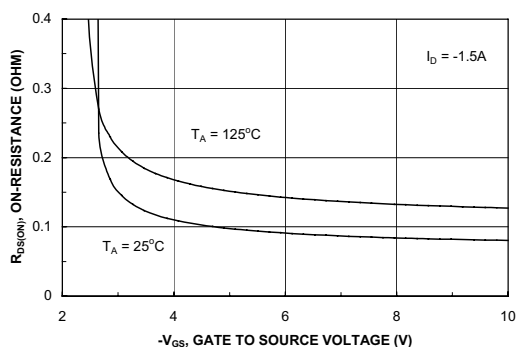


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

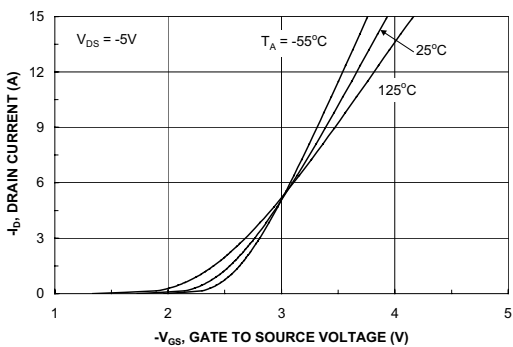


Figure 5. Transfer Characteristics.

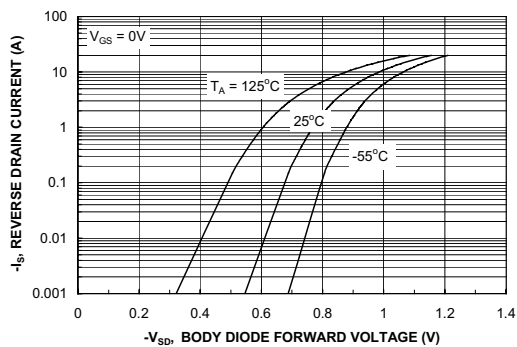


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-CH

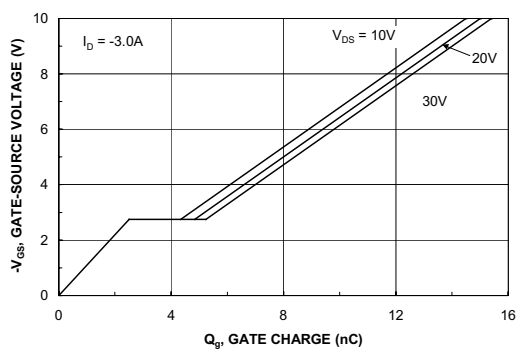


Figure 7. Gate Charge Characteristics.

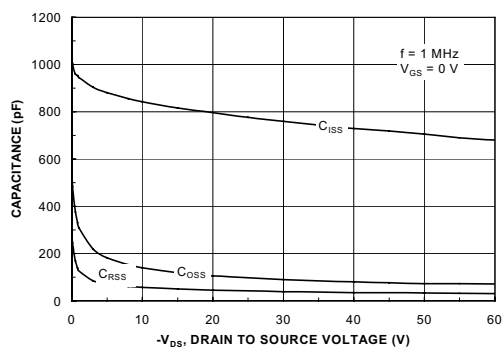


Figure 8. Capacitance Characteristics.

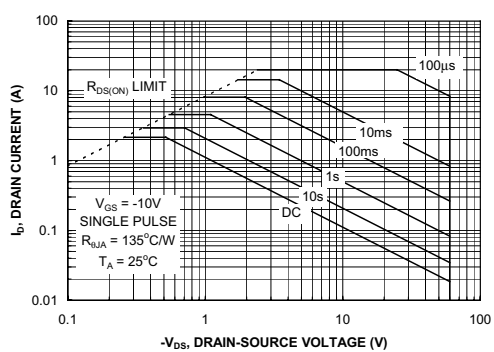


Figure 9. Maximum Safe Operating Area.

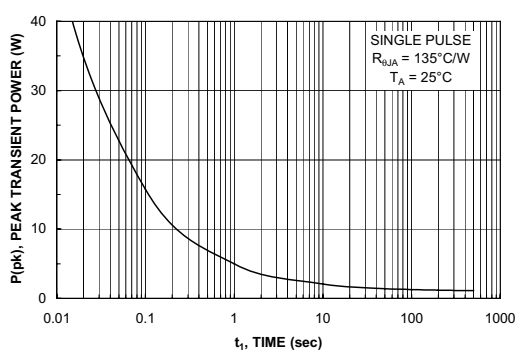


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N-CH

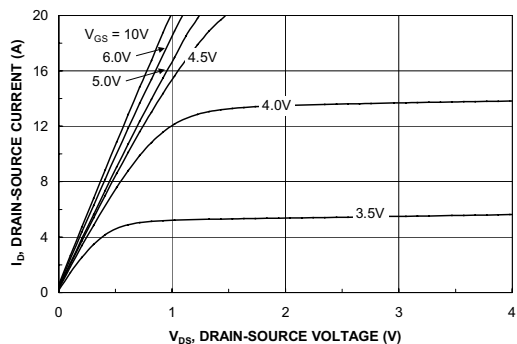


Figure 11. On-Region Characteristics.

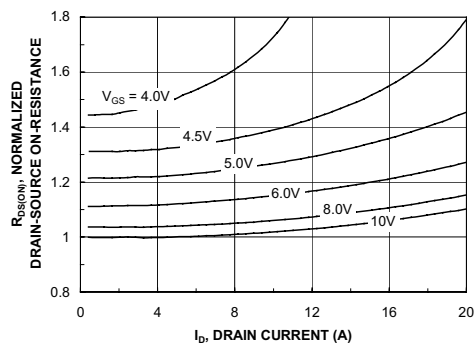


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

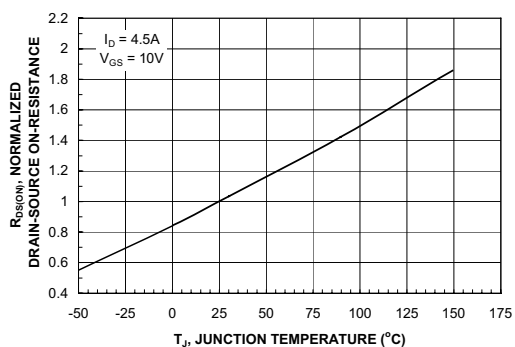


Figure 13. On-Resistance Variation with Temperature.

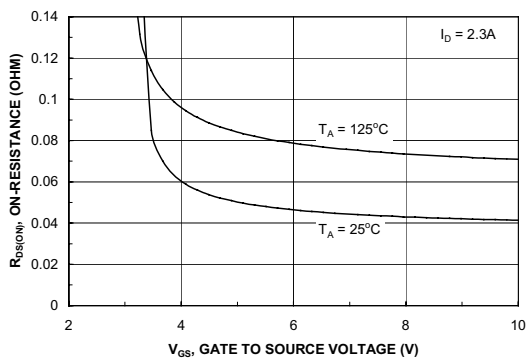


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

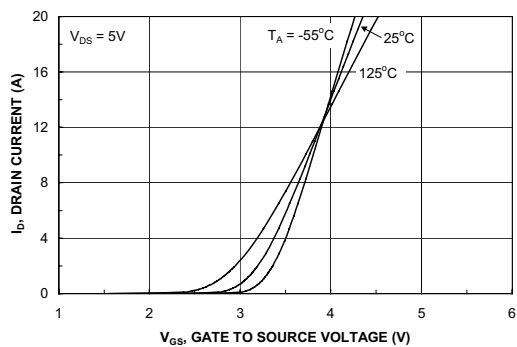


Figure 15. Transfer Characteristics.

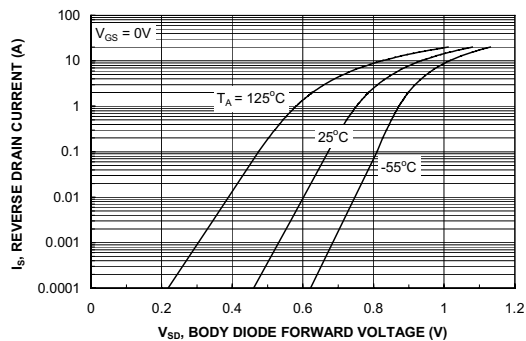


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-CH

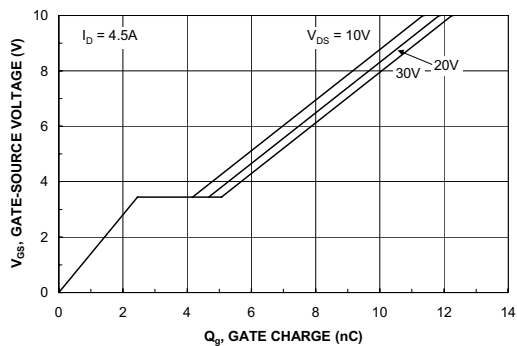


Figure 17. Gate Charge Characteristics.

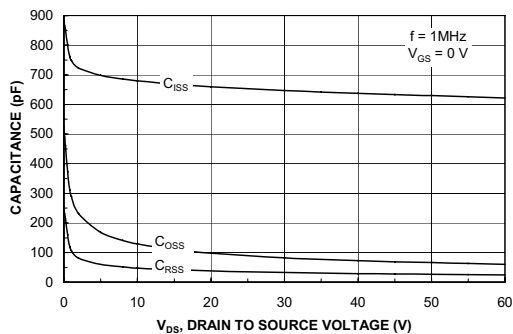


Figure 18. Capacitance Characteristics.

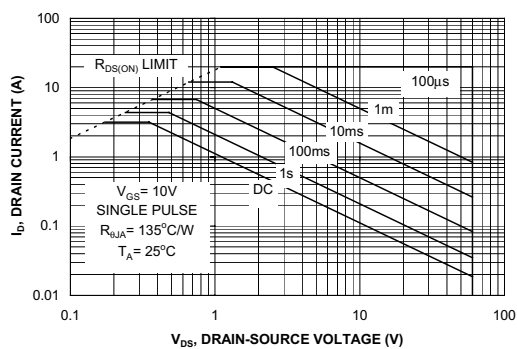


Figure 19. Maximum Safe Operating Area.

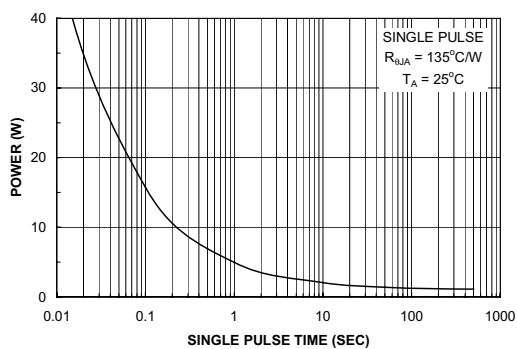


Figure 20. Single Pulse Maximum Power Dissipation.

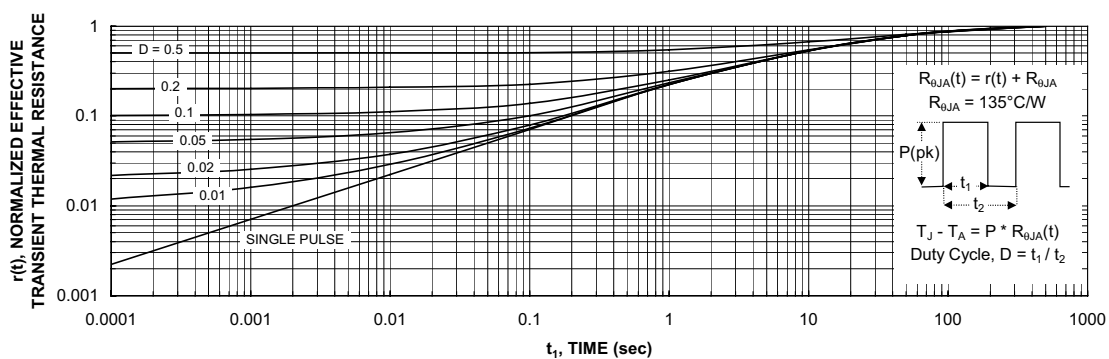
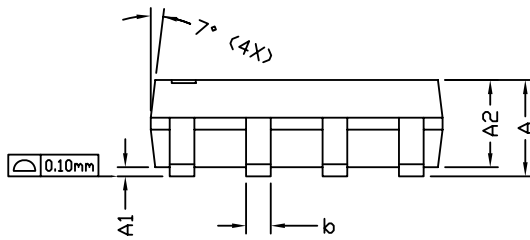
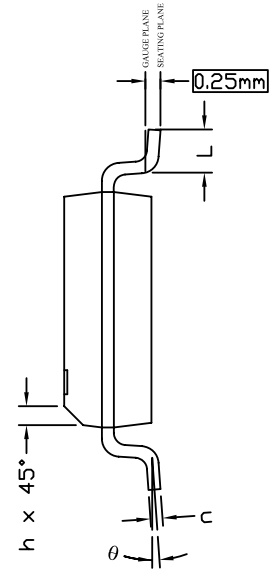
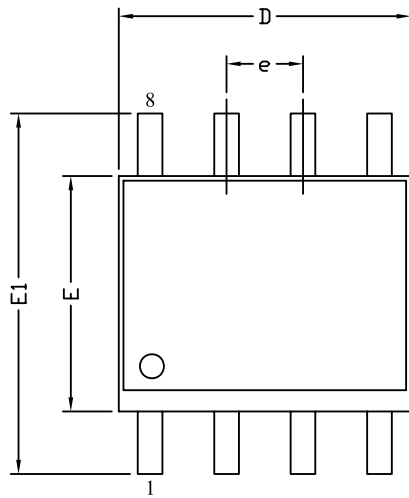


Figure 21. Transient Thermal Response Curve.

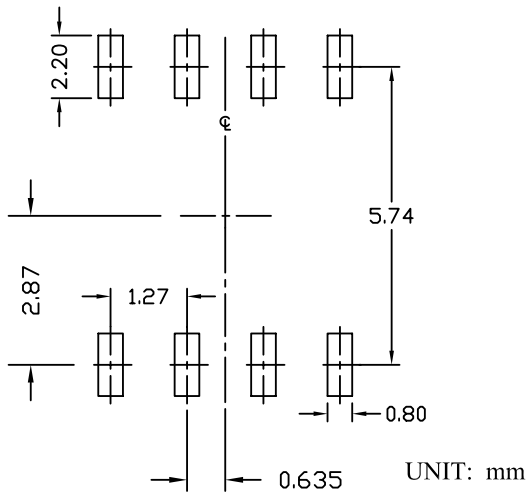
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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Version	rev H

S08 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	---	0.51	0.012	---	0.020
c	0.17	---	0.25	0.007	---	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	---	0.50	0.010	---	0.020
L	0.40	---	1.27	0.016	---	0.050
theta	0°	---	8°	0°	---	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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 - 2) 植埋于人体使用的装置。
 - 3) 用于治疗(切除患部、给药等)的装置。
 - 4) 其他直接影响到人的生命的装置。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.