

MT6401A

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{DS(ON)} (mΩ) Typ
-30V	-5A	47@ V _{GS} = -10V
		60@ V _{GS} = -4.5V
		80@ V _{GS} = -2.5V

Features

- Super high dense cell design for low R_{DS(ON)}
- Rugged and reliable
- Simple drive requirement
- SOT-26 package

Applications

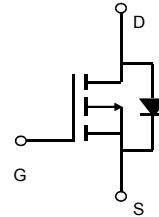
- Portable battery packs



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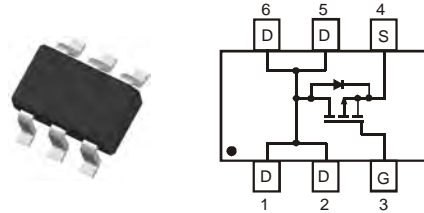
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

Top View



Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current-Continuous ^a @T _j =125°C	I _D	-5	A
	I _{DM}	-50	A
- Pulse ^d			
Drain-source Diode Forward Current ^a	I _S	-1.7	A
Maximum Power Dissipation ^a	P _D	1.25	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to Ambient ^a	R _{th JA}	80	°C/W
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ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±12V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	-0.5	-0.8	-1.1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-5A		47	50	mΩ
		V _{GS} =-4.5V, I _D =-3A		60	65	
		V _{GS} =-2.5V, I _D =-2A		80	85	
Forward Transconductance	g _{FS}	V _{GS} =-5V, I _D =-5A		5		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} =-10V, V _{GS} =0V f=1.0MHz		608		pF
Output Capacitance	C _{OSS}			115		pF
Reverse Transfer Capacitance	C _{RSS}			86		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =-10V I _D =-5A, V _{GEN} =-4.5V R _L =10ohm R _{GEN} =10ohm		10		ns
Rise Time	t _r			14		ns
Turn-Off Delay Time	t _{D(OFF)}			39		ns
Fall Time	t _f			26		ns
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-1A V _{GS} =-4.5V		9.2		nC
Gate-Source Charge	Q _{gs}			1.6		nC
Gate-Drain Charge	Q _{gd}			2.6		nC

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage	VSD	VGS=0V, IS=-1.7A		-0.84	-1.3	V

Notes

- a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$
- b. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- c. Guaranteed by design, not subject to production testing.

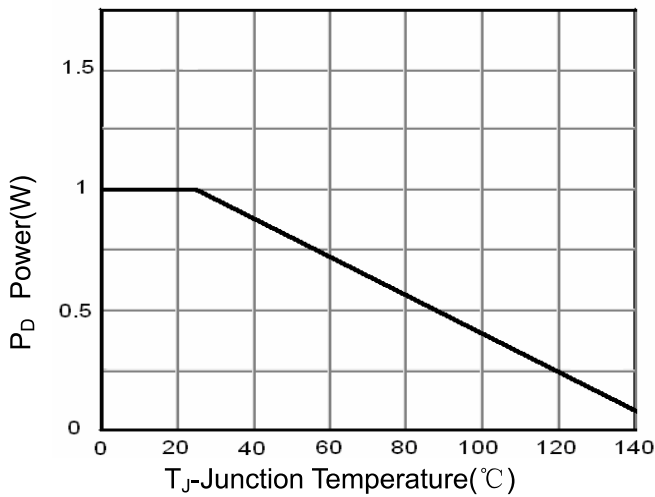


Figure 3 Power Dissipation

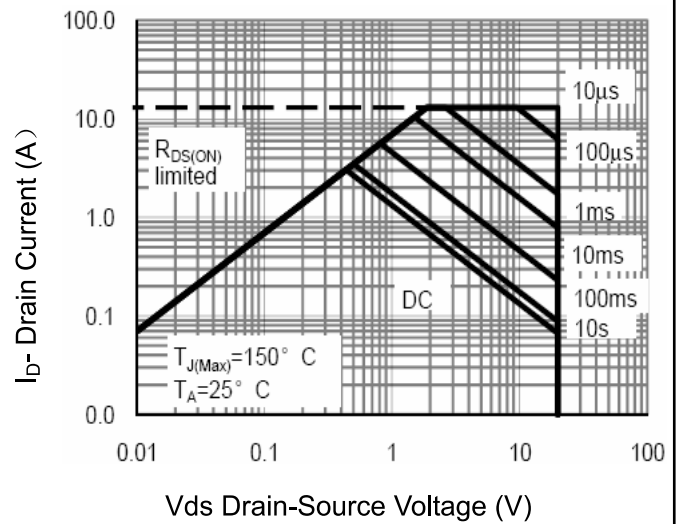


Figure 4 Safe Operation Area

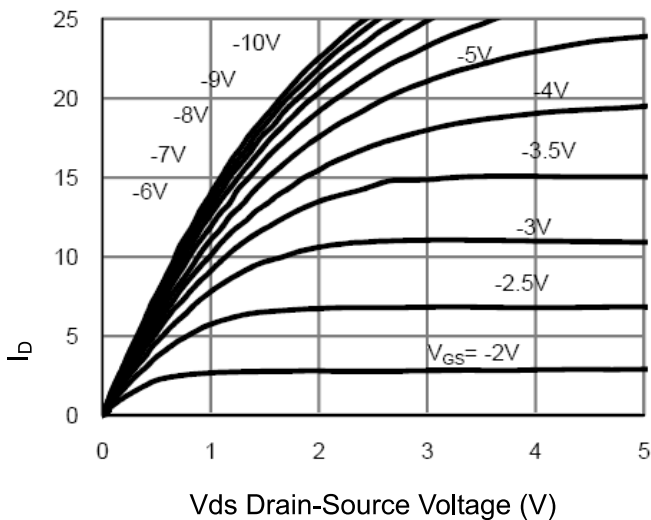


Figure 5 Output Characteristics

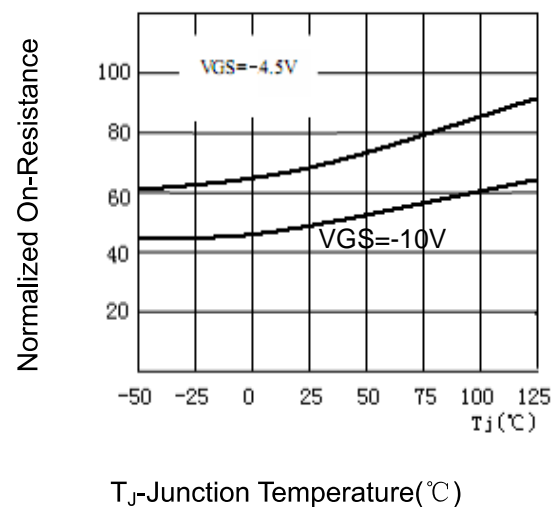


Figure 8 Drain-Source On-Resistance

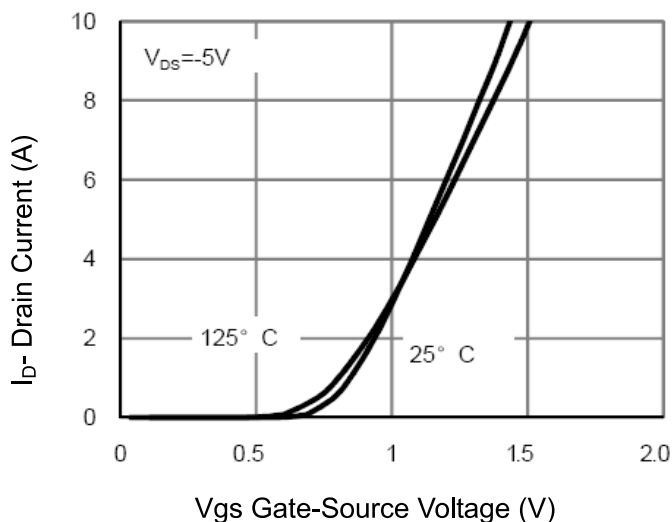


Figure 7 Transfer Characteristics

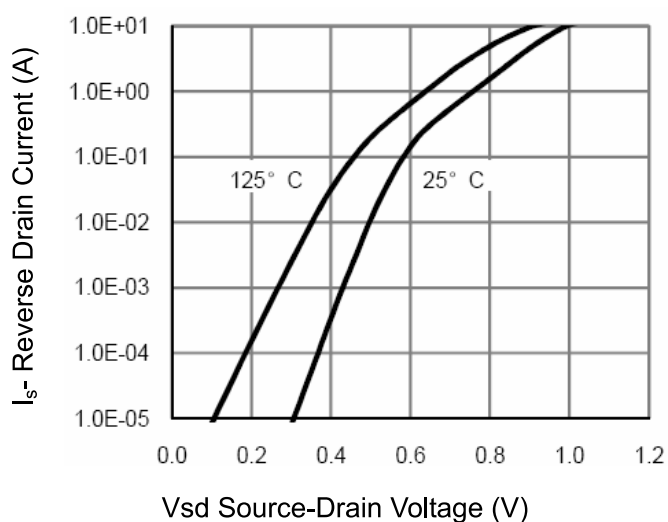


Figure 12 Source-Drain Diode Forward

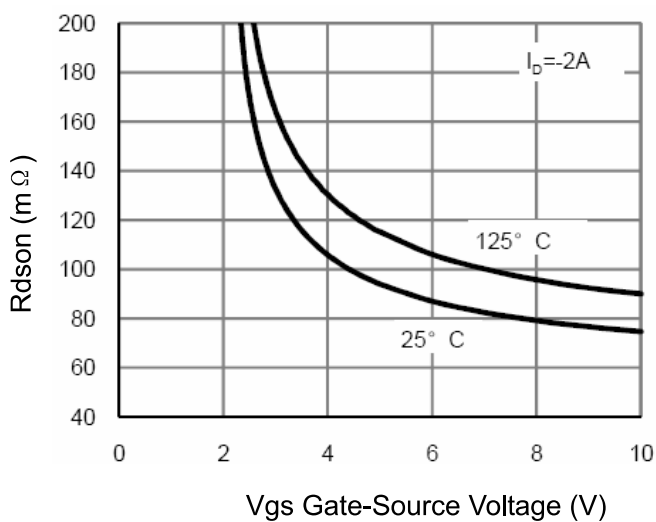


Figure 9 Rds(on) vs Vgs

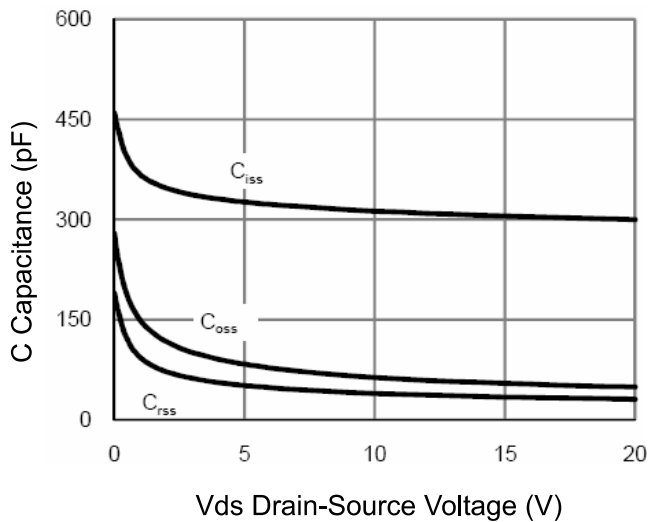


Figure 10 Capacitance vs Vds

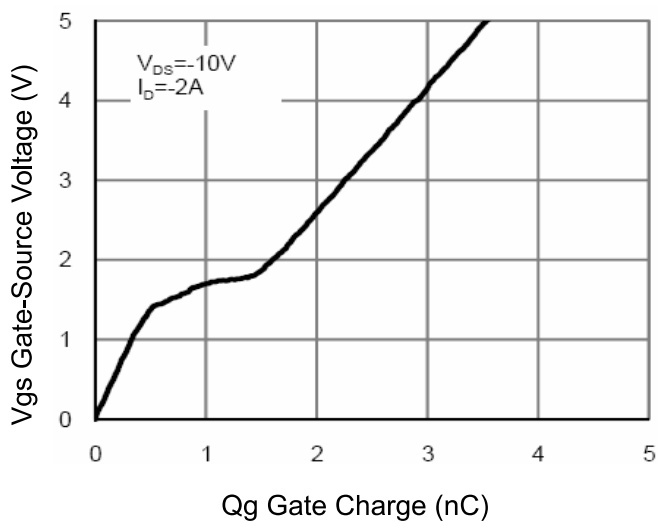
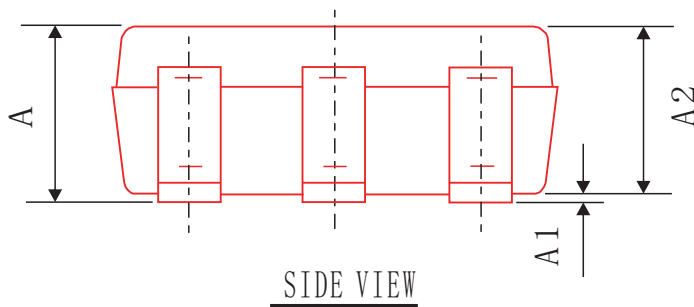
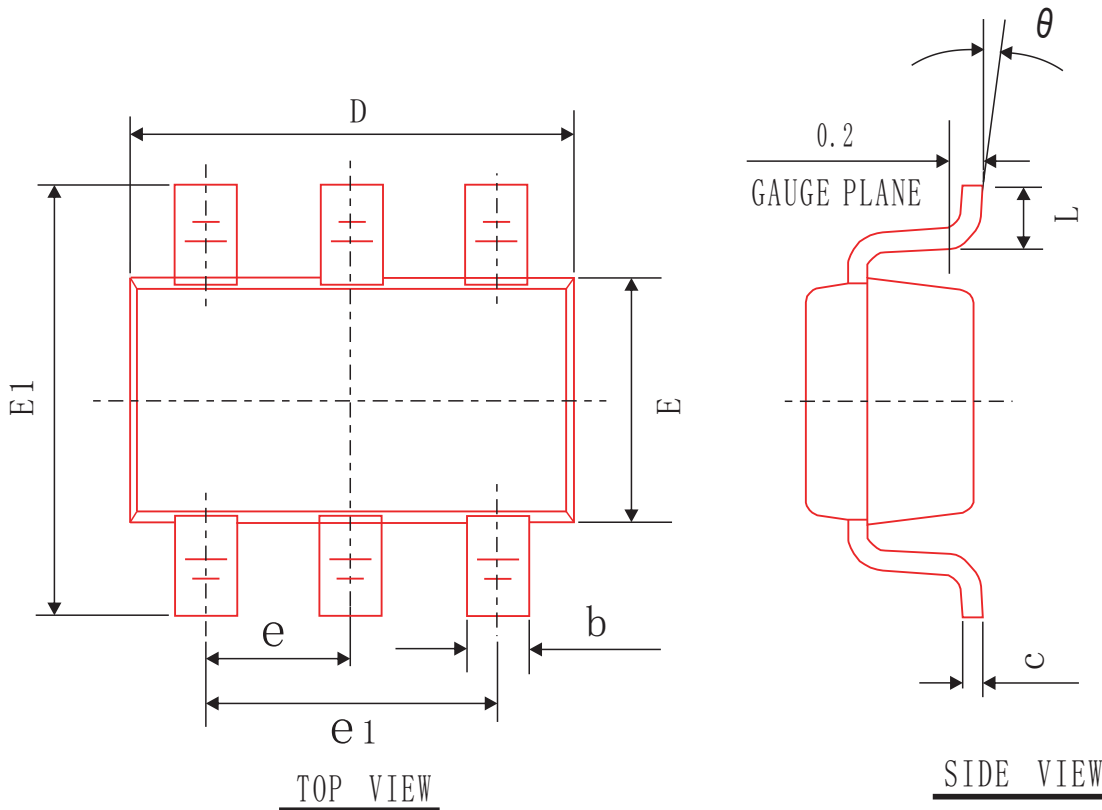


Figure 11 Gate Charge



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	---	---	1.20
A1	0.00	0.05	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.10	0.125	0.15
e1	1.80	1.90	2.00
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
L	0.30	0.45	0.60
θ	0°	4°	8°
e	0.95BSC		

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
2. DIMENSION "L" IS MEASURED IN GAGE PLANE.
3. TOLERANCE ± 0.100 mm(4 mil) UNLESS OTHERWISE SPECIFIED.
4. FOLLOWED FROM JEDEC MO-178C & MO-193C.
5. CONTROLLING DIMENSIONS IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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