# MT6968

# N-Channel Enhancement Mode Field Effect Transistor

## **Product Summary**

PRODUCT SUMMARY		
Vdss	ID R <sub>DS(ON)</sub> (mΩ) Typ	
20V	6.5A -	18@ V <sub>GS</sub> =4.5V
		23 @ V <sub>GS</sub> =2.5V
ESD Protected: 3000 V		

# Features

- Super high dense cell design for low RDS(ON)
- Rugged and reliable
- Simple drive requirement
- TSSOP-8 package

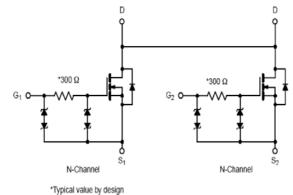
### Applications

Portable battery packs



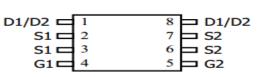
http://www.mtsemi.com

### **Simplified Schematic**



MARKING DIAGRAM & PIN ASSIGNMENT





TSSOP-8

# Absolute Maximum Ratings (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	MOSFET	Units
Drain-Source Voltage	Vds	20	V
Gate-Source Voltage	Vgs	±12	V
Continuous Drain Current <sup>A</sup>	ld	6.5	Α
Pulsed Drain Current <sup>B</sup>	lдм	30	А
Continuous Source Current (Diode Conduction)a	ls	1.5	А
Power Dissipation	PD	1.5	W
Junction and Storage Temperature Range	Тл, Тята	-55 to 150	°C

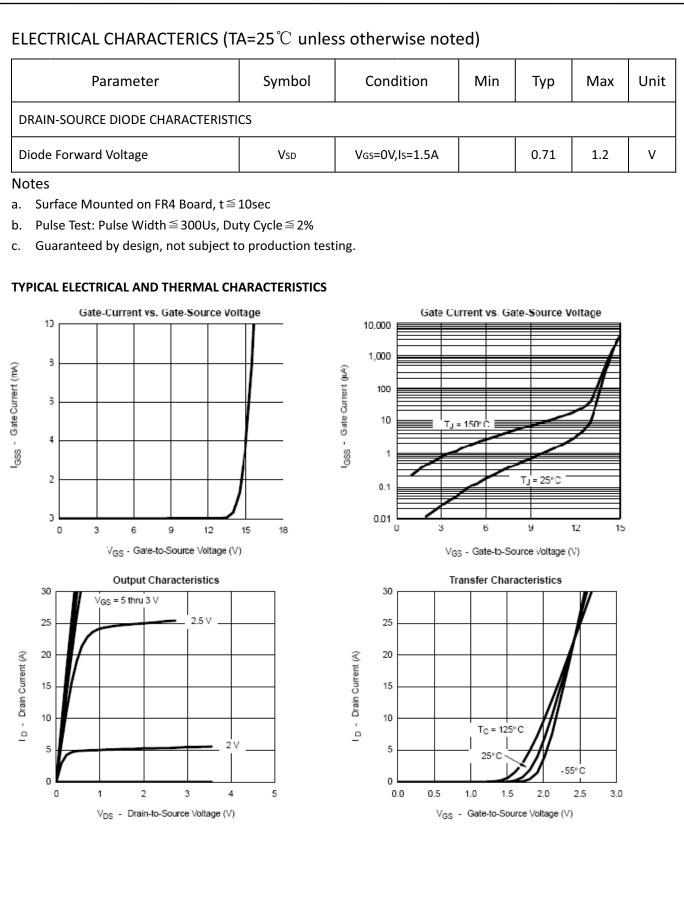
# THERMAL CHARACTERISTICS

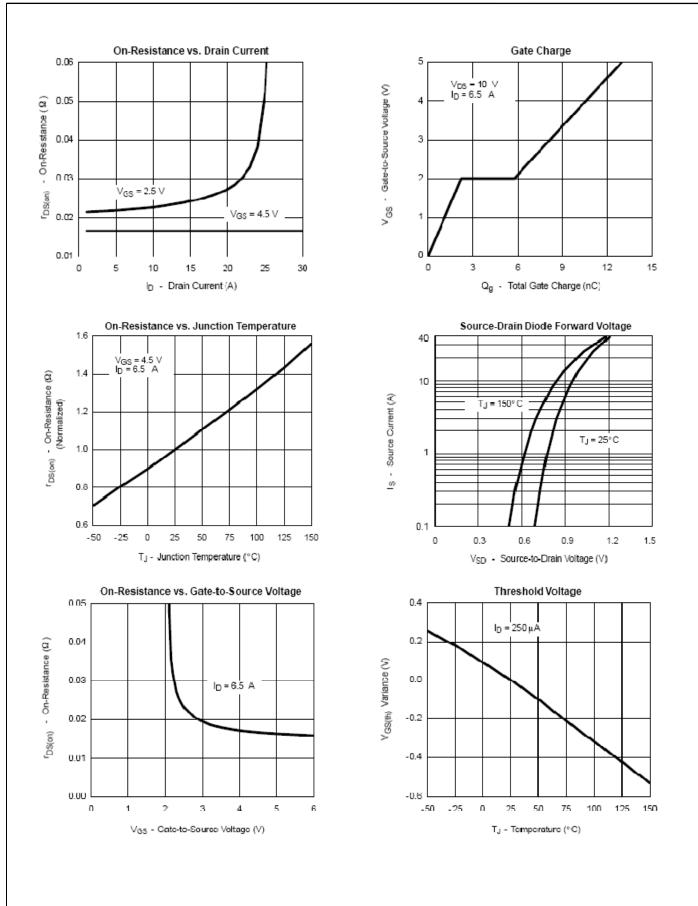
Thermal Resistance, Junction-to Ambient <sup>a</sup>	Rth JA	70	°C <b>∕W</b>	
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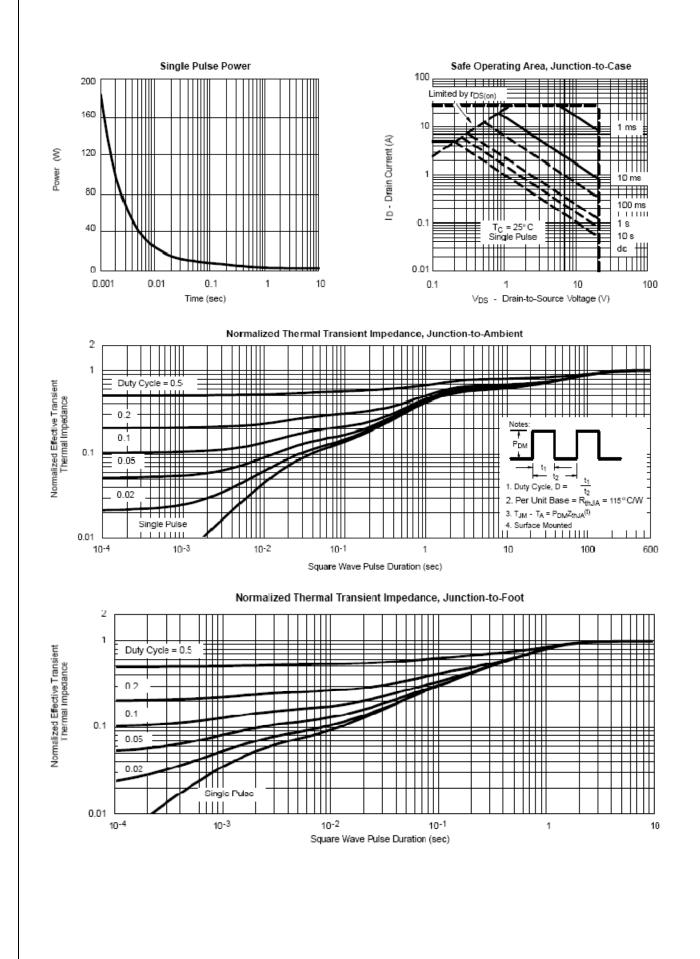
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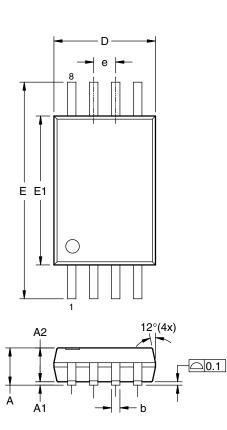
# ELECTRICAL CHARACTERISTICS (Ta=25 $^\circ\!\mathrm{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS			11		1	1
Drain-Source Breakdown Voltage	BVDSS	Vgs=0V,Id=-250µA	20			V
Zero Gate Voltage Drain Current	ldss	VDS=-16V,VGS=0V			1	μΑ
Gate-Body Leakage	lgss	Vgs=±8V,Vds=0V			±200	nA
ON CHARACTERITICS						
Gate Threshold Voltage	Vgs(th)	Vds=Vgs,Id=-250µA	0.8	1.0	1.2	V
Drain-Source On-State Resistance	Destaut	Vgs=4.5V,Id=6.5A		18	23	mΩ
	Rds(on)	Vgs=2.5V,Id=5.5A		23	28	
Forward Transconductance	gfs	Vgs=5V,Id=6.5A		30		S
DAYNAMIC CHARACTERISTICS					1	I
Input Capacitance	Ciss			540		pF
Output Capacitance	Coss	Vds=-10V,Vgs=0V f=1.0MHz		72		pF
Reverse Transfer Capacitance	Crss	1-1.000112		49		pF
SWITCHING CHARACTERISISTICS					1	I
Turn-On Delay Time	td(on)	VDD=10V		245		ns
Rise Time	tr	ID=1A,		330		ns
Turn-Off Delay Time	td(off)	V <sub>GEN</sub> =4.5V R∟=10ohm		860		ns
Fall Time	tf	Rgen=60hm		510		ns
Total Gate Charge	Qg			12	18	nC
Gate-Source Charge	Qgs	VDS=10V,ID=6.5A VGS=4.5V		2.2		nC
Gate-Drain Charge	Qgd	V G3-4.J V		3.6		nC

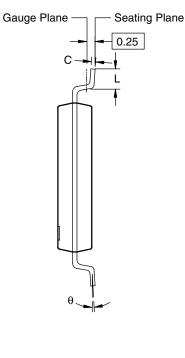




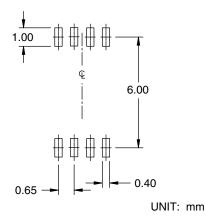




# **TSSOP-8** Package Dimensions



### **RECOMMENDED LAND PATTERN**



### **Dimensions in millimeters**

Symbols	Min.	Nom.	Max.
Α	_	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	_	0.30
С	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
е	0.65 BSC		
L	0.45	0.60	0.75
θ	<b>0</b> °	—	<b>8</b> °

### **Dimensions in inches**

Symbols	Min.	Nom.	Max.
Α		_	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	_	0.012
С	0.004	—	0.008
D	0.114	0.118	0.122
Е	0.252 BSC		
E1	0.169	0.173	0.177
е	0.026 BSC		
L	0.018	0.024	0.030
θ	<b>0</b> °	_	8°

#### Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions are inclusive of plating
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
- 4. Dimension L is measured in gauge plane.
- 5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
- 6. Refer to JEDEC MO-153(AA).

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