

MT81P65M5

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = -15V$
- $I_D = -80A$
- $R_{DS(ON)} = 4.0m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} = 5.0m\Omega @ V_{GS} = -2.5V$

Features

Advanced Trench Process Technology.

- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

Applications

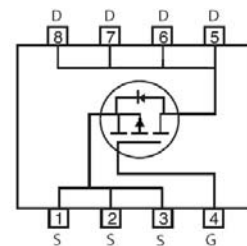
- Notebook Computer
- Portable Battery Pack



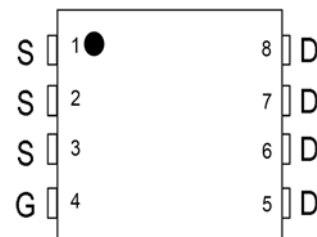
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



DFN5X6-8L

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-15	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-80	A
Drain Current-Pulsed <small>(Note 1)</small>	I_{DM}	-240	A
Maximum Power Dissipation	P_D	36	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <small>(Note 2)</small>	$R_{\theta JA}$	40	$^\circ C/W$
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Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT81P65M5	MT81P65M5	DFN5X6-8L	7"	8mm	3000 units

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-15	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.7	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-20A$	-	4.0	5.0	m Ω
		$V_{GS}=-2.5V, I_D=-10A$	-	5.0	6.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-15A$	30	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{ISS}	$V_{DS}=-12V, V_{GS}=0V,$ $F=1.0MHz$	-	2910	-	PF
Output Capacitance	C_{OSS}		-	420	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	280	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-10A,$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	16	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	21	-	nS
Total Gate Charge	Q_g	$V_{DS}=-12V, I_D=-10A, V_{GS}=-10V$	-	48	-	nC
Gate-Source Charge	Q_{gs}		-	12	-	nC
Gate-Drain Charge	Q_{gd}		-	14	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-8A$	-	-	-0.7	V

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Characteristics Curve ($T_A=25^\circ\text{C}$, unless otherwise noted)

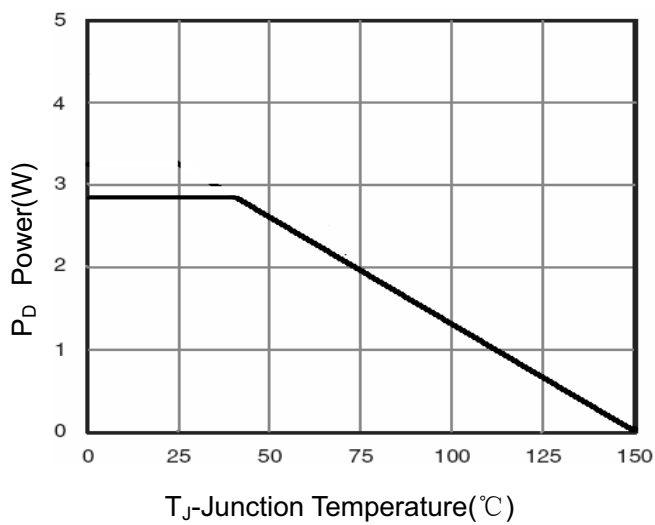


Figure 1 Power Dissipation

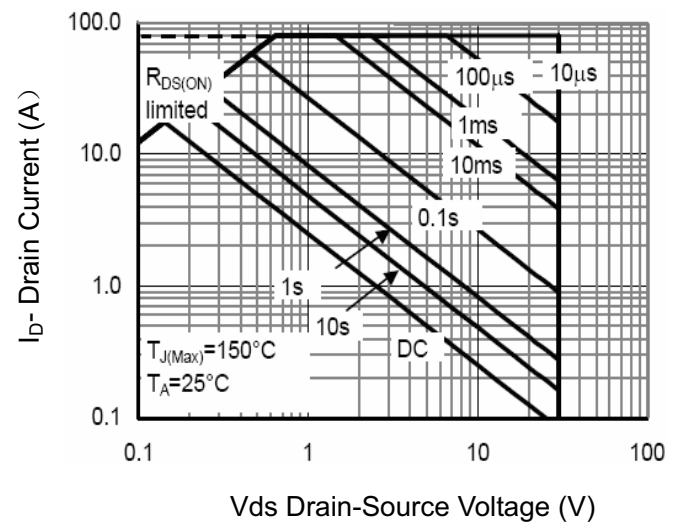


Figure 2 Safe Operation Area

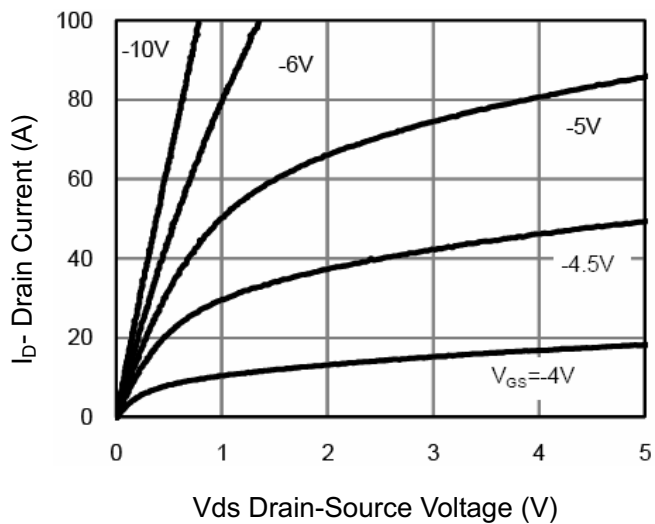


Figure 3 Output Characteristics

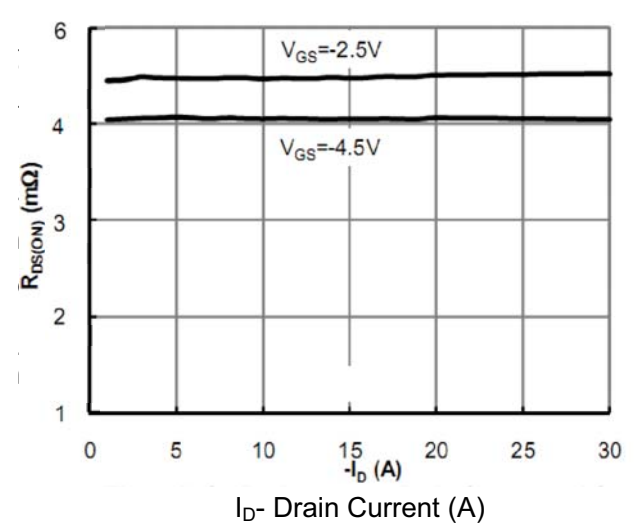


Figure 4 Drain-Source On-Resistance

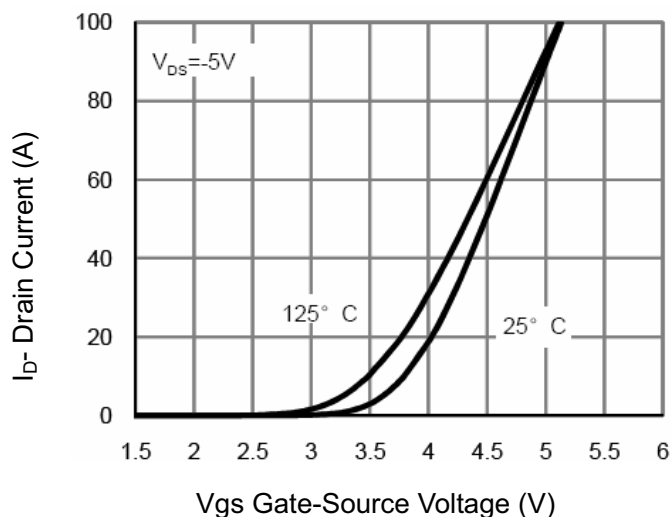


Figure 5 Transfer Characteristics

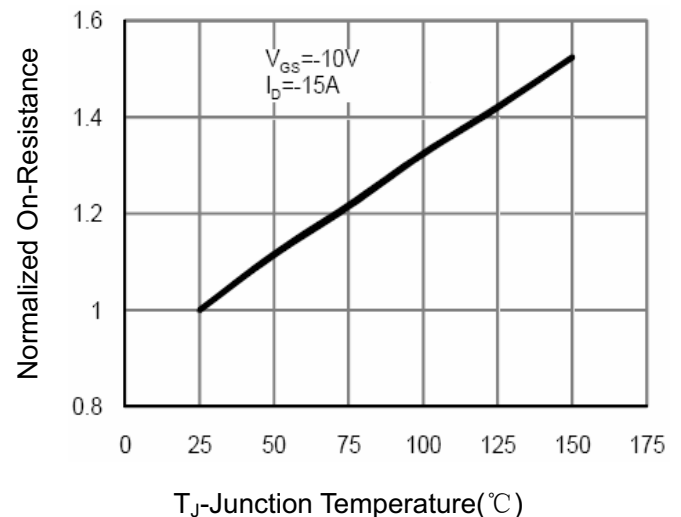


Figure 6 Drain-Source On-Resistance

Characteristics Curve ($T_A=25^\circ\text{C}$, unless otherwise noted)

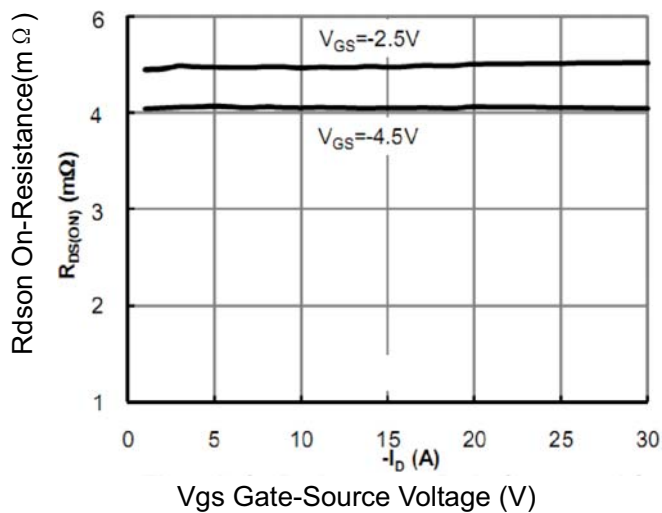


Figure 7 $R_{DS(on)}$ vs V_{GS}

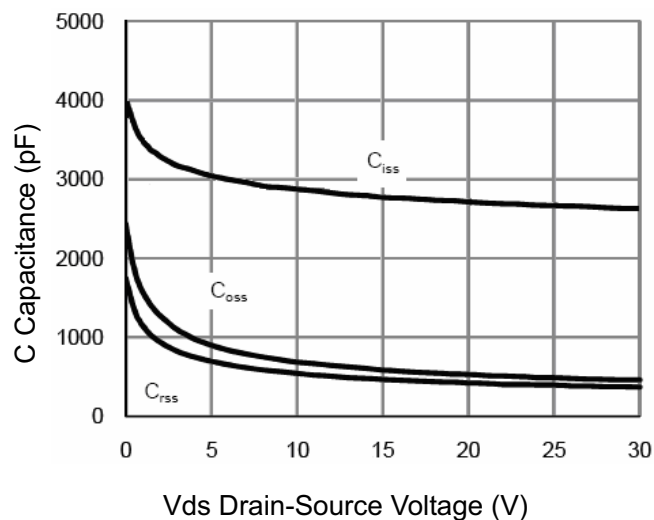


Figure 8 Capacitance vs V_{DS}

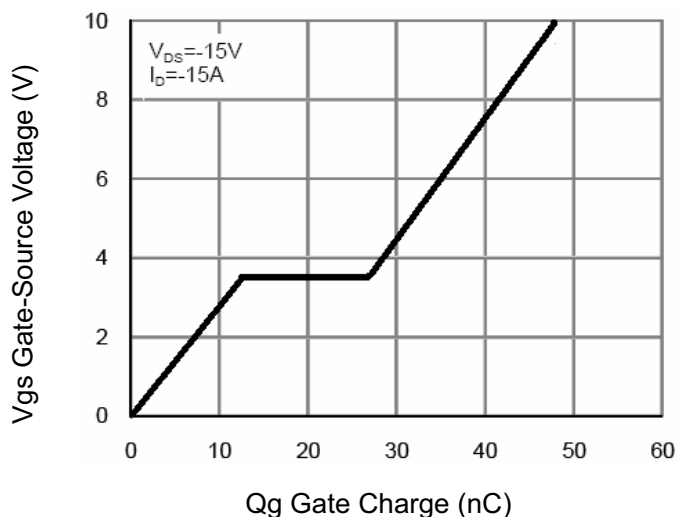


Figure 9 Gate Charge

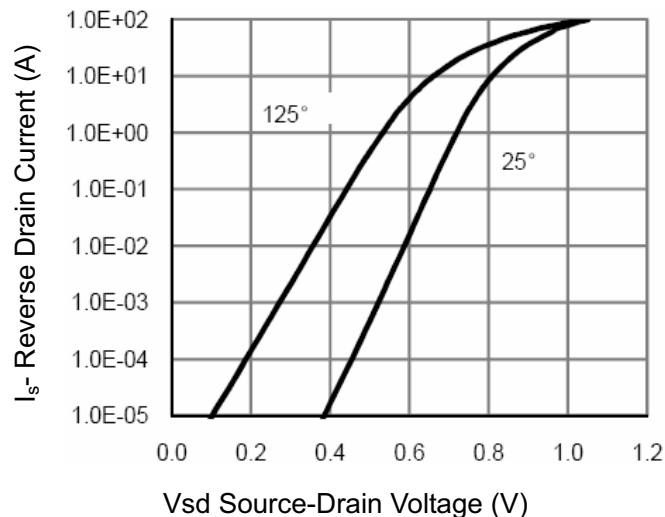


Figure 10 Source- Drain Diode Forward

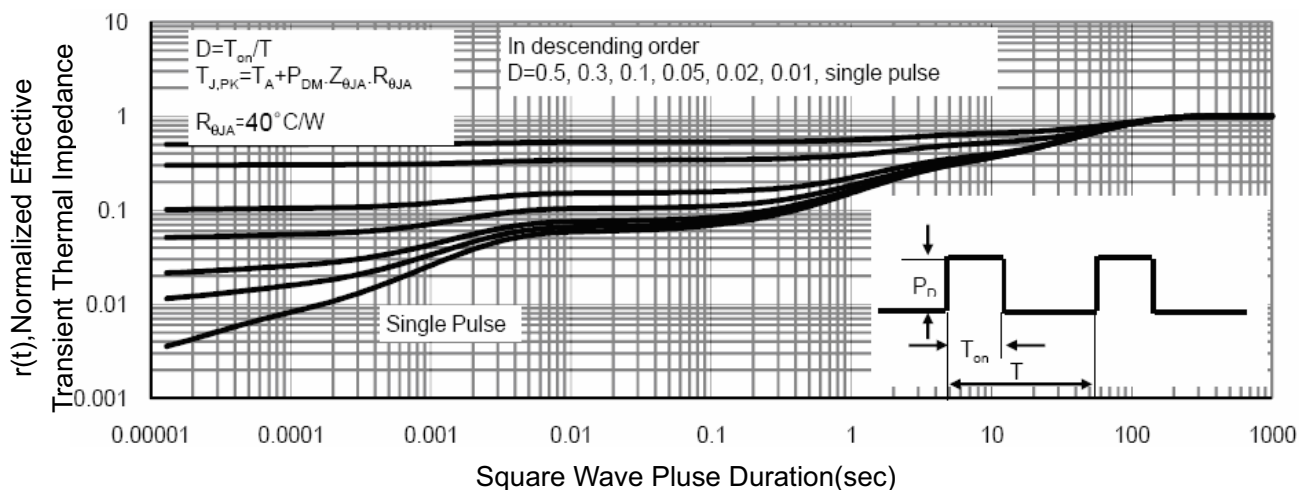
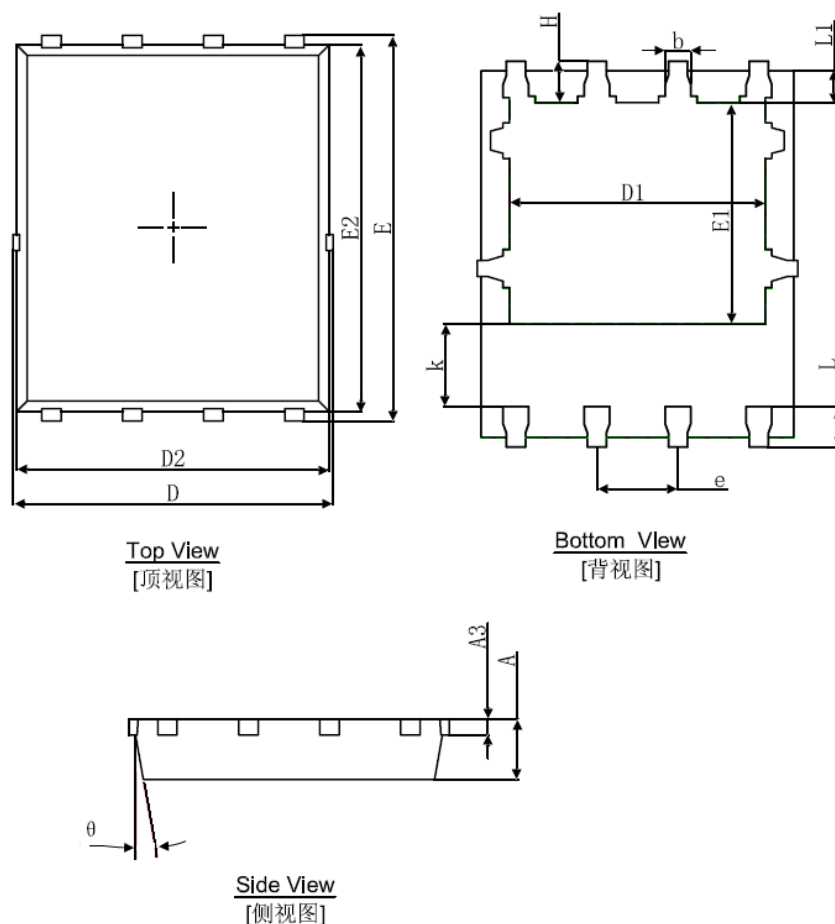


Figure 11 Normalized Maximum Transient Thermal Impedance

PDFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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