MT8205A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

PRODUCT SUMMARY					
V _{DSS}	ID	$Rds(ON)$ $(m \Omega)$ Typ			
20V	6A	20 @ VGS=4.5V			
		28 @ VGS=2.5V			

Features

- Super high dense cell design for low RDS(ON)
- · Rugged and reliable
- · Simple drive requirement
- · TSSOP-8 package

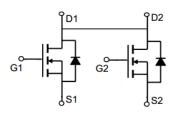
Applications

· Portable battery packs



http://www.mtsemi.com

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

Top View

D1/D2 🗖 1	8 🗖 D1/D2
S1 🗖 2	7 🗖 S2
S1 🗖 3	6 🗖 S2
G1 □ 4	5 🗖 G2

Absolute Maximum Ratings(T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	Vgs	±12	V
Drain Current-Continuous ^a @Tj=125°C	ID	6	A
- Pulse d ^b	Ірм	20	A
Drain-source Diode Forward Current ^a	Is	1.7	A
Maximum Power Dissipation ^a	PD	2.5	W
Operating Junction and Storage Temperature Range	Tj,Tstg	-55 to 150	$^{\circ}$ C

THERMAL CHARACTERISTICS

Thermal Resistance, Junetion to Timolent	Thermal Resistance, Junction-to Ambient ^a	Rth JA	80	°C/W
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ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

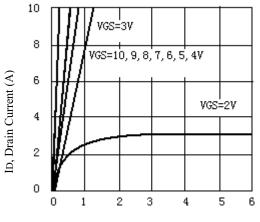
Parameter	Symbol	Condition	Min	Тур	Max	Uni	
OFF CHARACTERISTICS	Symoor	Condition	IVIIII	Тур	IVIAX	Cili	
of the determination of the second of the se			1				
Drain-Source Breakdown Voltage	BVDSS	$V_{GS}=0V,I_{D}=250\mu A$	20			V	
Zero Gate Voltage Drain Current	Idss	$V_{DS}=16V, V_{GS}=0V$			1	μД	
Gate-Body Leakage	Igss	$V_{GS}=\pm 8V, V_{DS}=0V$			±100	nA	
ON CHARACTERITICS							
Gate Threshold Voltage	Vgs(th)	$V_{DS}=V_{GS},I_{D}=250\mu A$	0.5	0.7	1.5	V	
Durin Corres On Chata Braintain	Dragon	V _{GS} =4.5V,I _D =6A		20	23	- C	
Drain-Source On-State Resistance	Rds(on)	V _{GS} =2.5V,I _D =2.8A		28	35	mΩ	
Forward Transconductance	gFS	V _{GS} =5V,I _D =5A		5		S	
DYNAMIC CHARACTERISTICS						•	
Input Capacitance	Ciss			608		pF	
Output Capacitance	Coss	$V_{DS}=10V, V_{GS}=0V$ f=1.0MHz		115		pF	
Reverse Transfer Capacitance	Crss	1 1.0WIIIZ		86		pF	
SWITCHING CHARACTERISISTICS					1		
Turn-On Delay Time	td(ON)	V _{DD} =10V		10		ns	
Rise Time	tr	ID=6A,		14		ns	
Turn-Off Delay Time	tD(OFF)	V _{GEN} =4.5V R _L =10ohm		39		ns	
Fall Time	tf	R _{GEN} =10ohm		26		ns	
Total Gate Charge	Qg			9.2		nC	
Gate-Source Charge	Qgs	VDS=10V,ID=1A VGS=4.5V		1.6		пC	
Gate-Drain Charge	Qgd	v us-4.3 v		2.6		пC	

ELECTRICAL CHARACTERICS (TA=25 C unless otherwise noted)

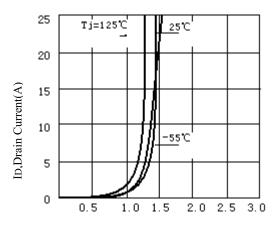
Parameter	Symbol	Condition	Min	Тур	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage	Vsd	V _{GS} =0V,I _S =1.7A		0.84	1.3	V

Notes

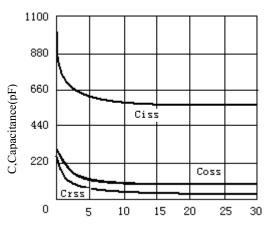
- a. Surface Mounted on FR4 Board, t ≤ 10sec
- b. Pulse Test: Pulse Width ≤ 300Us, Duty Cycle ≤ 2%
- c. Guaranteed by design, not subject to production testing.



VDS, Drain-to-Source Voltage (V) Figure 1. Output Characteristics



VGS, Gate-to-source Voltage (V) Figure 2. Transfer Characteristics



VGS, Drain-to Source Voltage

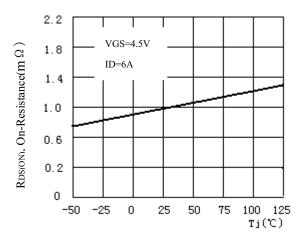
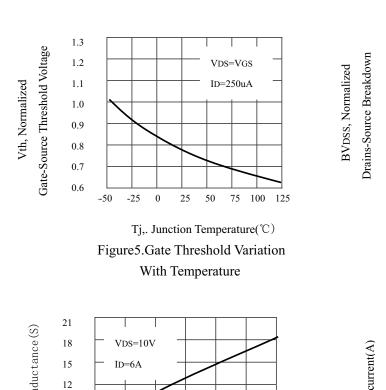
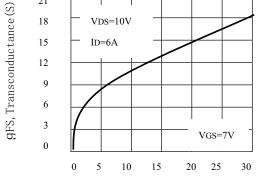


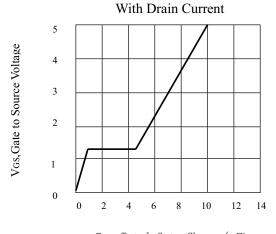
Figure 4. On-Resistance Variation with $\label{eq:condition} Temperature$

Figure 3. Capacitance

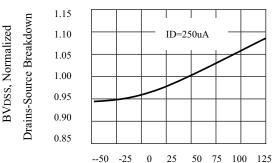




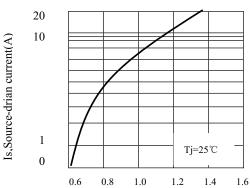
IDS, Drain-Source Current (A)
Figure 7. Transconductance Variation



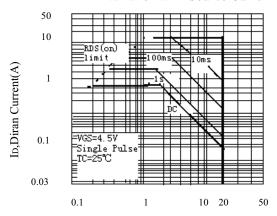
Qg, Total Gate Charge (nC) Figure 9. Gate Charge



Tj, .Junction Temperature ($^{\circ}$ C)
Figure 6.Breakdown Voltage Variation
With Temperature

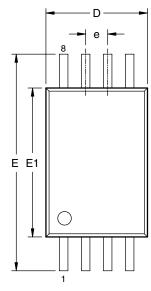


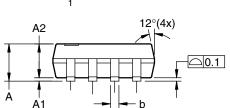
Vsp, Body Diode Forward Voltage Figure8.Body Diode Forward Voltage Variation with Source Current

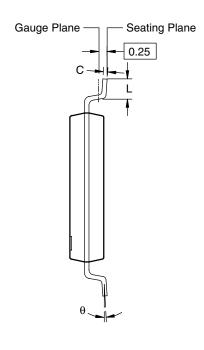


VDS, Drain-Source Voltage(V)
Figure 10.Maximum Safe Operating Area

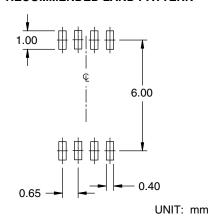
TSSOP-8 Package Dimensions







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.		
Α	_	_	1.20		
A1	0.05	_	0.15		
A2	0.80	1.00	1.05		
b	0.19	_	0.30		
С	0.09	_	0.20		
D	2.90	3.00	3.10		
E	6.40 BSC				
E1	4.30	4.40	4.50		
е	0.65 BSC				
L	0.45	0.60	0.75		
θ	0°	_	8°		

Dimensions in inches

Min.	Nom.	Max.		
		0.047		
0.002		0.006		
0.031	0.039	0.041		
0.007	_	0.012		
0.004		0.008		
0.114	0.118	0.122		
0.252 BSC				
0.169	0.173	0.177		
0.026 BSC				
0.018	0.024	0.030		
0°	_	8°		
		0.002 - 0.031 0.039 0.007 - 0.004 - 0.114 0.118 0.252 BS0 0.169 0.173 0.026 BS0 0.018 0.024		

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions are inclusive of plating
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
- 4. Dimension L is measured in gauge plane.
- 5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
- 6. Refer to JEDEC MO-153(AA).

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