N-Channel Enhancement Mode Field Effect Transistor

Product Summary

PRODUCT S	SUMMARY	
Vdss	ID $RDS(ON) (m \Omega) Ty$	
20V	6A	20 @ VGS=4.5V
		24 @ VGS=2.5V

Features

- Super high dense cell design for low RDS(ON)
- Rugged and reliable
- Simple drive requirement
- TSSOP-8 package

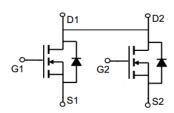
Applications

Portable battery packs



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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

Top View

D1/D2 🗖 1	8 🗖 D1/D2
S1 = 2	7 🗖 S2
S1 🗖 3	6 🗖 S2
G1 🗖 4	5 🗖 G2

Absolute Maximum Ratings(T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	Vds	20	V
Gate-Source Voltage	VGS	±12	V
Drain Current-Continuous ^a @Tj=25°C	ID	6	А
- Pulse d^b	Ідм	20	А
Drain-source Diode Forward Current ^a	Is	1.7	А
Maximum Power Dissipation ^a	PD	2.5	W
Operating Junction and Storage Temperature Range	Tj,Tstg	-55 to 150	°C

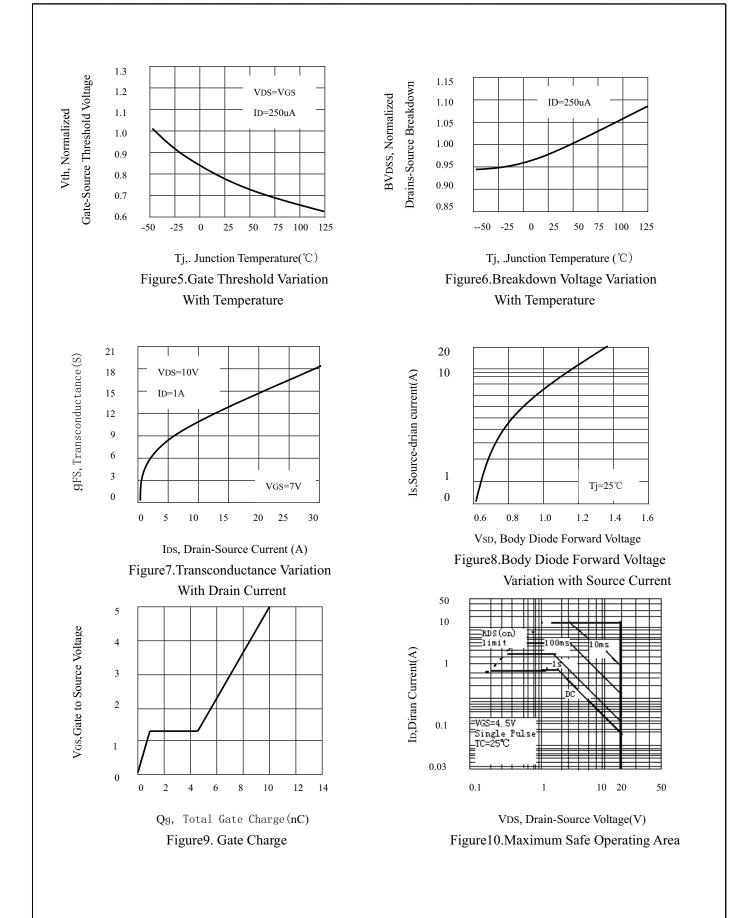
THERMAL CHARACTERISTICS

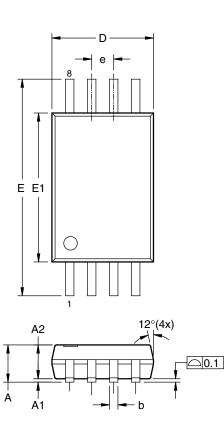
Thermal Resistance, Junction-to Ambient ^a	Rth JA	80	°C/W
	-		

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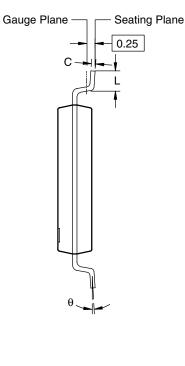
Parameter	Symbol	Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS			1	l	1	
Drain-Source Breakdown Voltage	BVDSS	Vgs=0V,Id=250µA	20			V
Zero Gate Voltage Drain Current	Idss	VDS=16V,VGS=0V			1	μA
Gate-Body Leakage	IGSS	V _{GS} =±8V,V _{DS} =0V			±100	nA
ON CHARACTERITICS						
Gate Threshold Voltage	VGs(th)	VDS=VGS,ID=250µA	0.5	0.7	1.1	V
Drain-Source On-State Resistance	_	VGS=4.5V,ID=3A		20	21	mΩ
	RDS(ON)	Vgs=2.5V,ID=0.8A		24	25	
Forward Transconductance	gfs	VGS=5V,ID=1A		5		S
DYNAMIC CHARACTERISTICS					1	
Input Capacitance	Ciss			608		pF
Output Capacitance	Coss	VDS=10V,VGS=0V f=1.0MHz		115		pF
Reverse Transfer Capacitance	Crss	I-1.0MHZ		86		pF
SWITCHING CHARACTERISISTICS					1	
Turn-On Delay Time	td(on)	VDD=10V		10		ns
Rise Time	tr	ID=6A,		14		ns
Turn-Off Delay Time	td(off)	VGEN=4.5V RL=100hm		39		ns
Fall Time	tf	RGEN=10ohm		26		ns
Total Gate Charge	Qg			9.2		nC
Gate-Source Charge	Qgs	VDS=10V,ID=1A		1.6		nC
Gate-Drain Charge	Qgd	V _{GS} =4.5V		2.6		nC

Parameter	Symbol	Condition	Min	Тур	Max	Un
DRAIN-SOURCE DIODE CHARAC	TERISTICS		.1	1	1	
Diode Forward Voltage	Vsd	Vgs=0V,Is=1.0A		0.8		V
Surface Mounted on FR4 Board, t Pulse Test: Pulse Width \leq 300Us, D Guaranteed by design, not subject to (V) $VGS=3VVGS=10, 9, 8, 7, 6(V)$ $GS=10, 9, 8, 7, 6(V)$ (V) $(V$	Puty Cycle $\leq 2\%$ o production testin 3, 5, 4V VGS=2V 4 5 6	25 Tj=125 20 15 10 10 10 0 5 0.5		2.0 2.		7)
VDS, Drain-to-Sour Figure 1. Output Ch (F_{d}) (Coss 20 25 30 ce Voltage	Figure 2. T	1 I I _D (A)	haracte	ristics =4.5V _ 2	

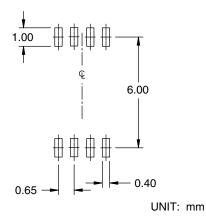




TSSOP-8 Package Dimensions



RECOMMENDED LAND PATTERN



Dimensions in millimeters

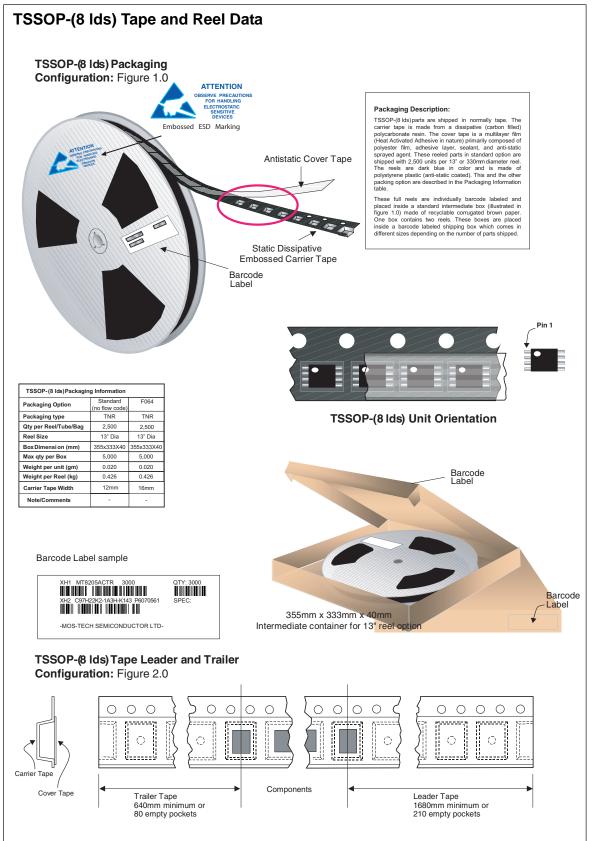
Symbols	Min.	Nom.	Max.
Α	_	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
С	0.09	—	0.20
D	2.90	3.00	3.10
Е	6.40 BSC		
E1	4.30	4.40	4.50
е	0.65 BSC		
L	0.45	0.60	0.75
θ	0 °	—	8 °

Dimensions in inches

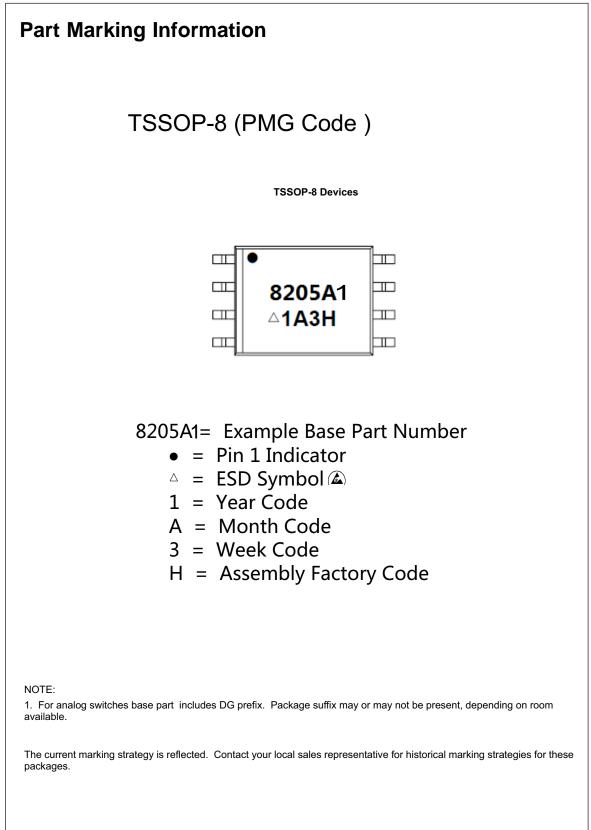
Symbols	Min.	Nom.	Max.
Α		—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	_	0.012
С	0.004	—	0.008
D	0.114	0.118	0.122
E	0.252 BSC		
E1	0.169	0.173	0.177
е	0.026 BSC		
L	0.018	0.024	0.030
θ	0°	_	8°

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions are inclusive of plating
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
- 4. Dimension L is measured in gauge plane.
- 5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
- 6. Refer to JEDEC MO-153(AA).

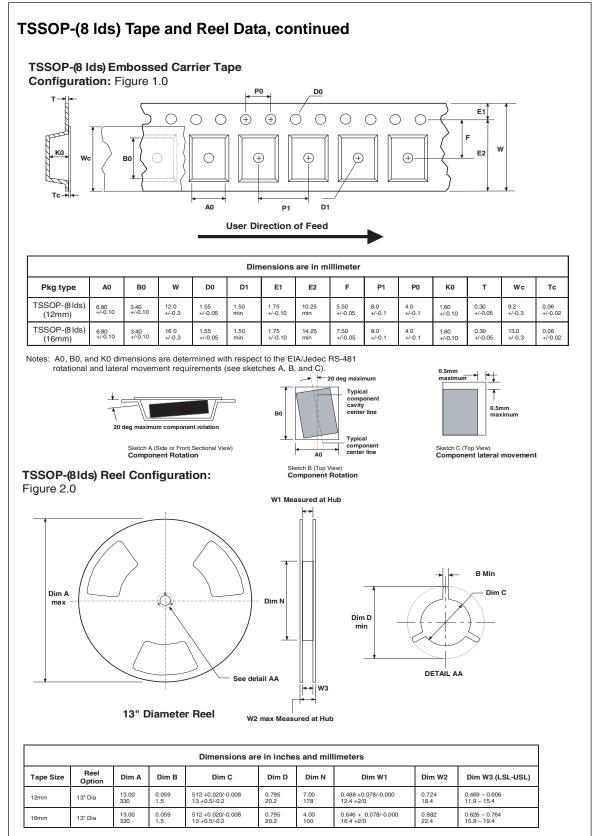


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