

MT8310N3

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = 30V$
- $I_D = 40A$
- $R_{DS(ON)} \leq 5 m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 6 m\Omega @ V_{GS}=4.5V$

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

Applications

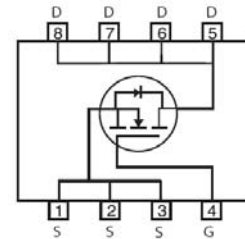
- Notebook Computer
- Portable Battery Pack



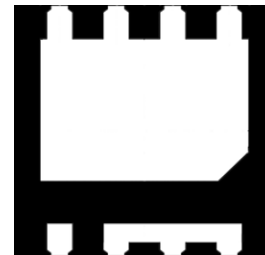
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



DFN3X3-8L

PIN1

Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted					
Parameter		Symbol	Maximum		Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current ^{AF}	$T_A=25^{\circ}C$	I_{DSM}	40		A
	$T_A=70^{\circ}C$		25		
Pulsed Drain Current ^B		I_{DM}	120		A
Avalanche Current ^C		I_{AR}	32		A
Repetitive avalanche energy $L=0.3mH^C$		E_{AR}	75		mJ
Power Dissipation	$T_A=25^{\circ}C$	P_{DSM}	2.8		W
	$T_A=70^{\circ}C$		1.6		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^{\circ}C$
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	32	40	$^{\circ}C/W$
Maximum Junction-to-Ambient ^A	Steady-State		60	75	$^{\circ}C/W$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	16	24	$^{\circ}C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =1mA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =85°C			1 100	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.7	1.3	2.0	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =15A		5.0		mΩ
		V _{GS} =4.5V, I _D =15A		6.0		mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		66		S
V _{SD}	Diode Forward Voltage	I _S =1.5A, V _{GS} =0V		0.7		V
I _S	Maximum Body-Diode + Schottky Continuous Current				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1840	2200	pF
C _{oss}	Output Capacitance			720		pF
C _{rss}	Reverse Transfer Capacitance			63		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.8	1.2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		27	33	nC
Q _g (4.5V)	Total Gate Charge			12	15	nC
Q _{gs}	Gate Source Charge			4.2		nC
Q _{gd}	Gate Drain Charge			4.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.2Ω, R _{GEN} =3Ω		5.5		ns
t _r	Turn-On Rise Time			5.5		ns
t _{D(off)}	Turn-Off DelayTime			25		ns
t _f	Turn-Off Fall Time			4.3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		14	17	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		30	36	nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

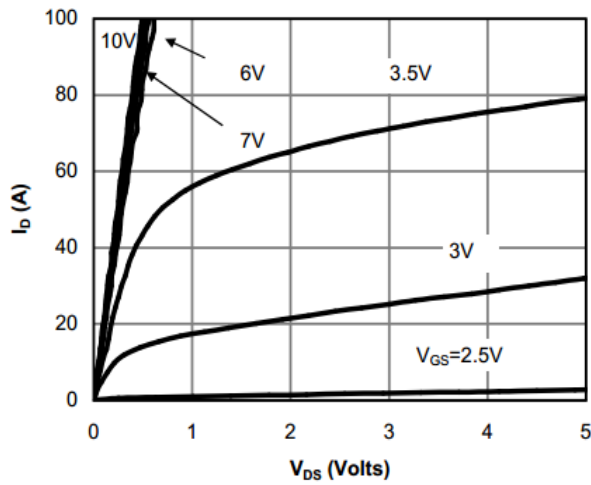


Fig 1: On-Region Characteristics (Note E)

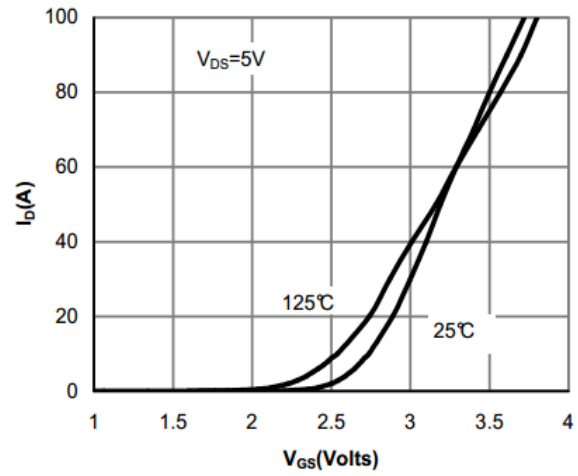


Figure 2: Transfer Characteristics (Note E)

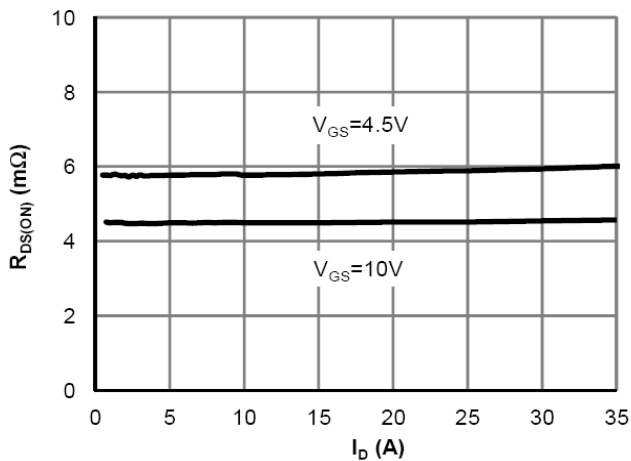


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

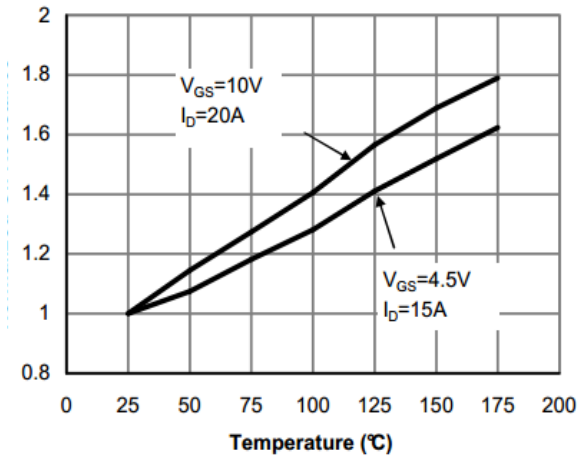


Figure 4: On-Resistance vs. Junction Temperature (Note E)

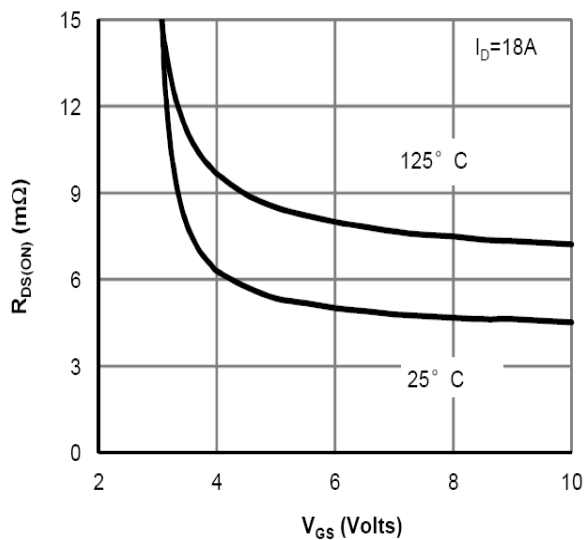


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

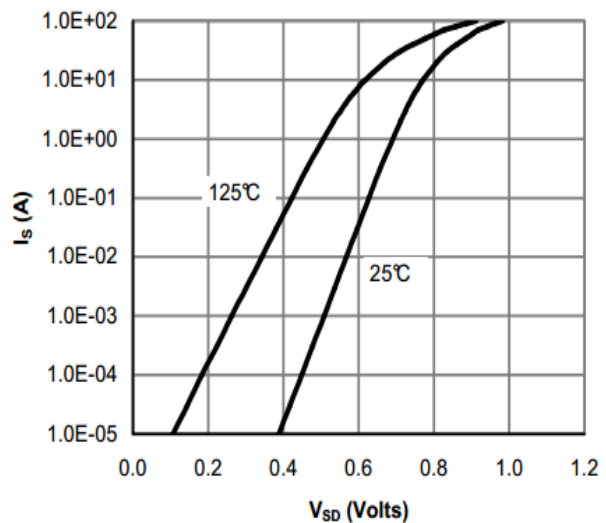


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

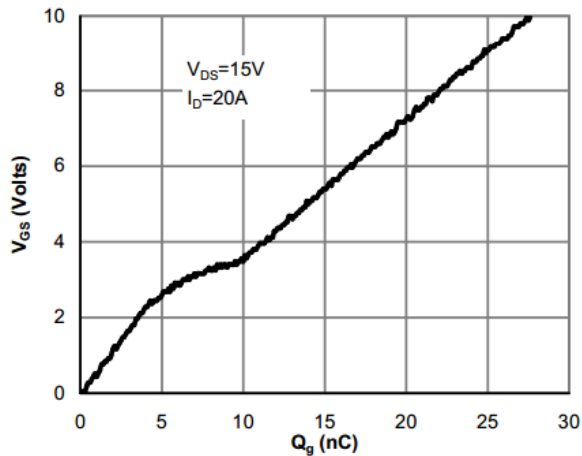


Figure 7: Gate-Charge Characteristics

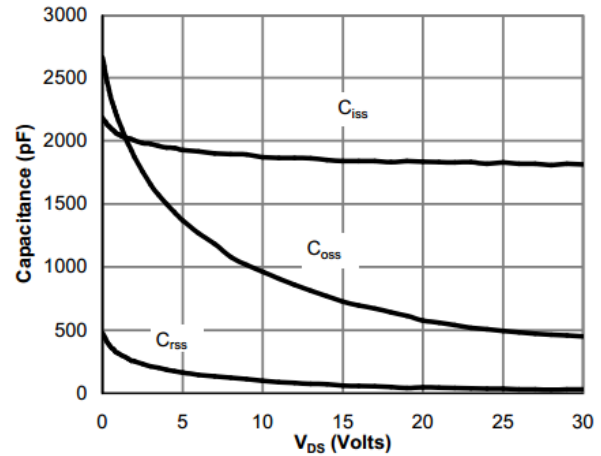


Figure 8: Capacitance Characteristics

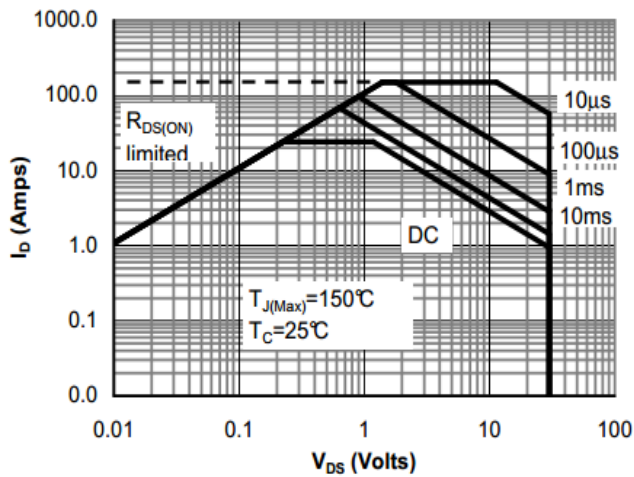


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

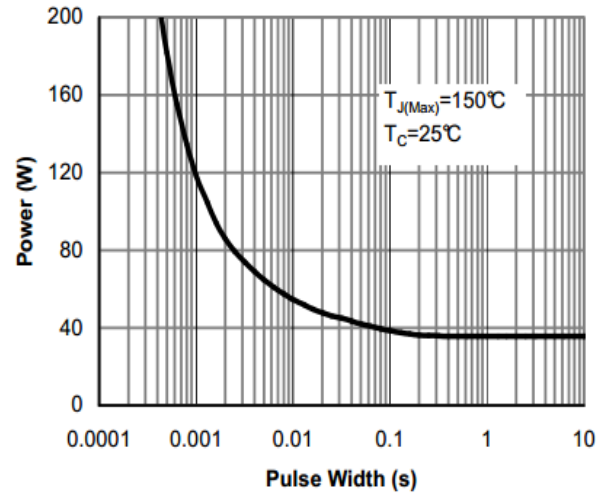


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

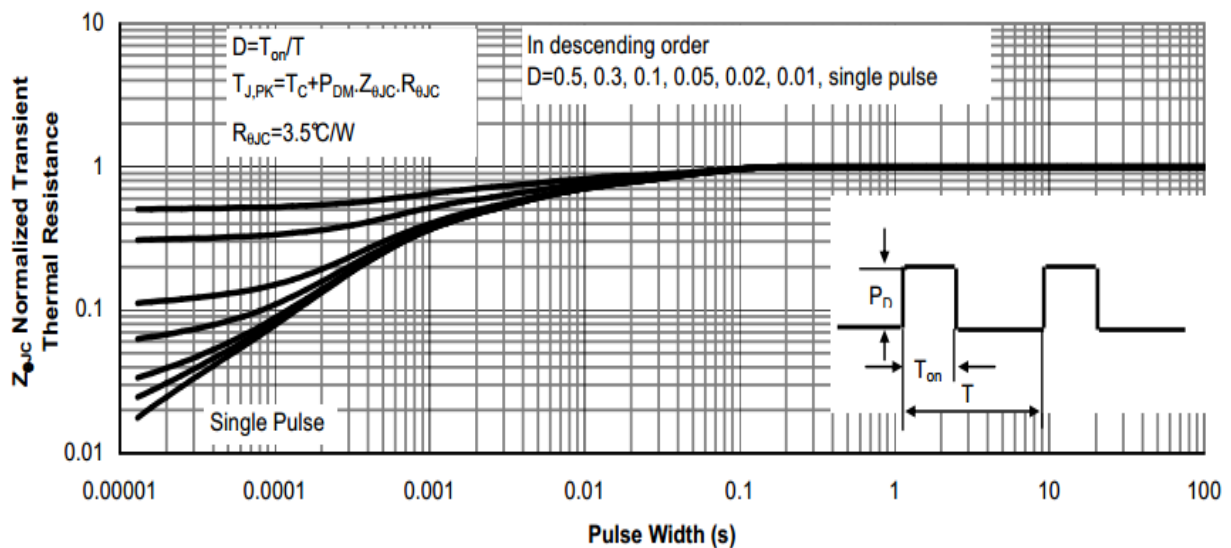
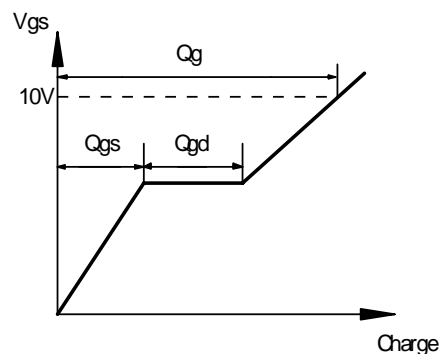
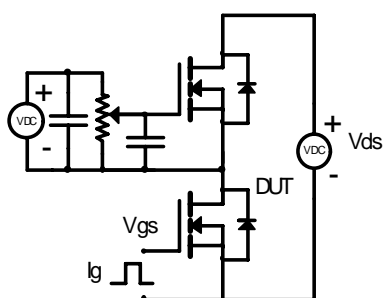
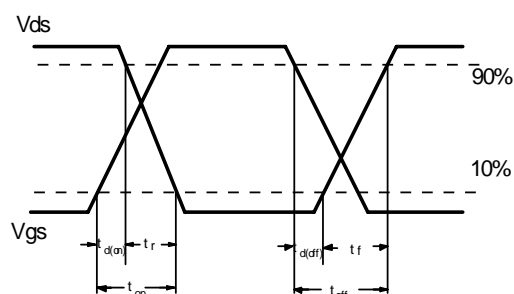
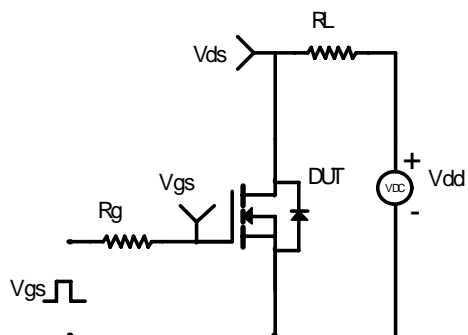


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

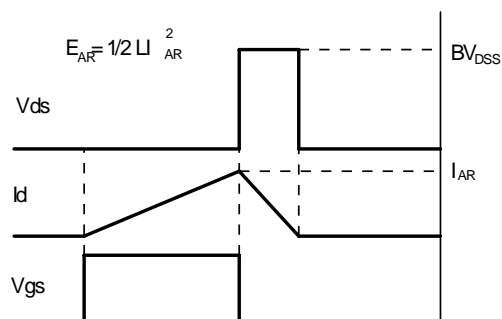
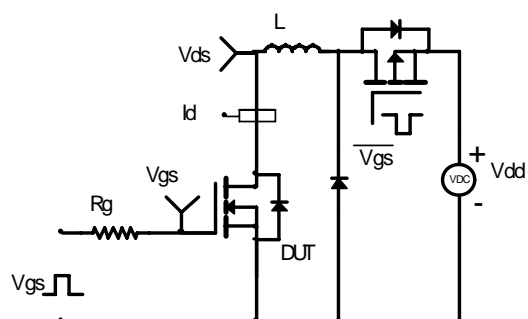
Gate Charge Test Circuit & Waveform



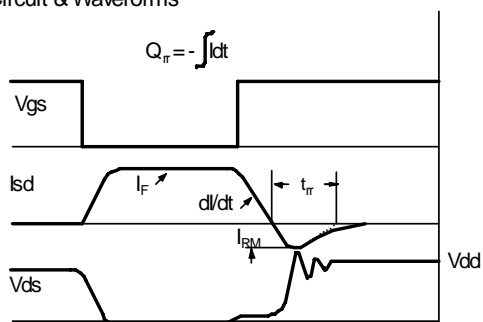
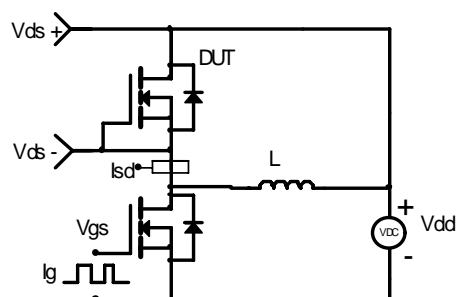
Resistive Switching Test Circuit & Waveforms



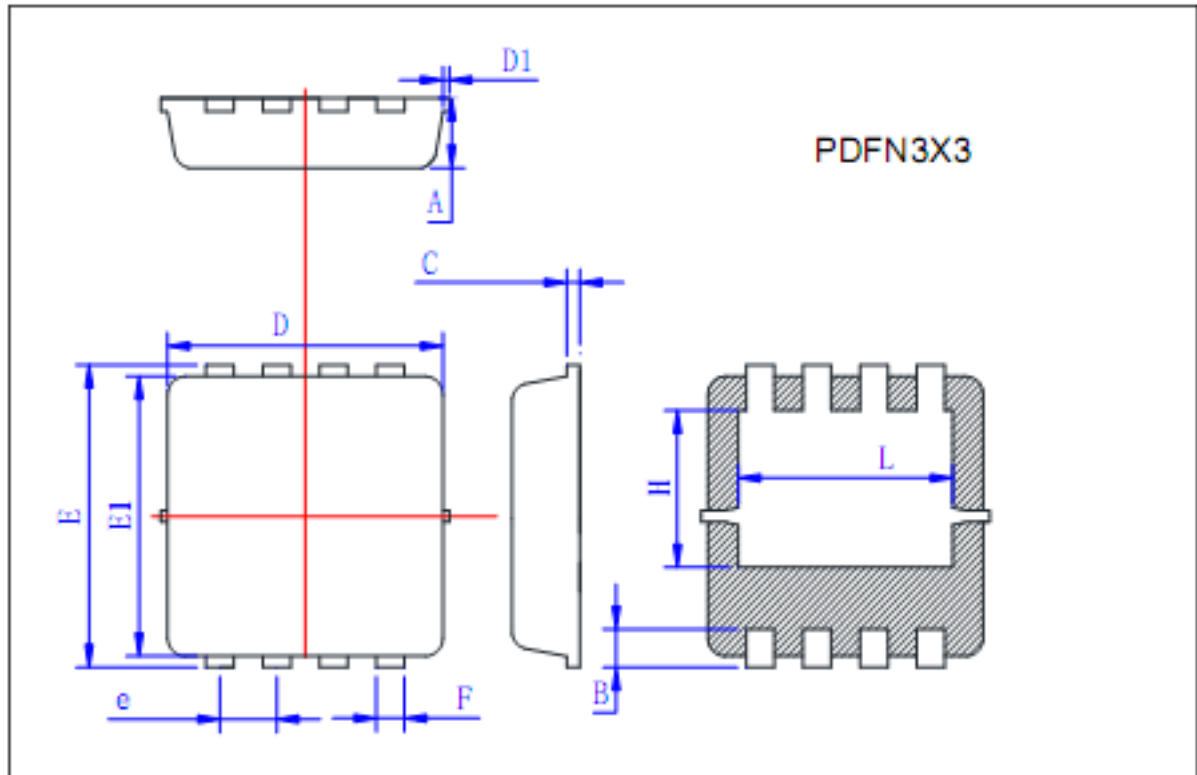
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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