

# MT8311M5

## N-Channel Enhancement Mode Power MOSFET

### Description

The MT8311M5 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

- $V_{DS} = 30V, I_D = 100A$   
 $R_{DS(ON)} < 1.9\ m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 2.9m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	100	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	70.7	A
Pulsed Drain Current	$I_{DM}$	300	A
Maximum Power Dissipation	$P_D$	65	W
Derating factor		0.43	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

### Package Marking and Ordering Information

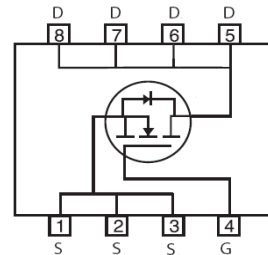
Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT8311M5	MT8311M5	DFN5X6-8L	-	-	-



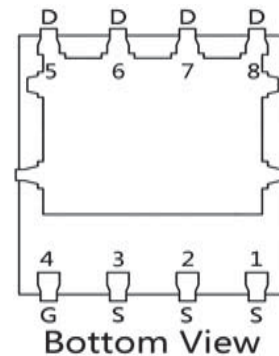
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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.3	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

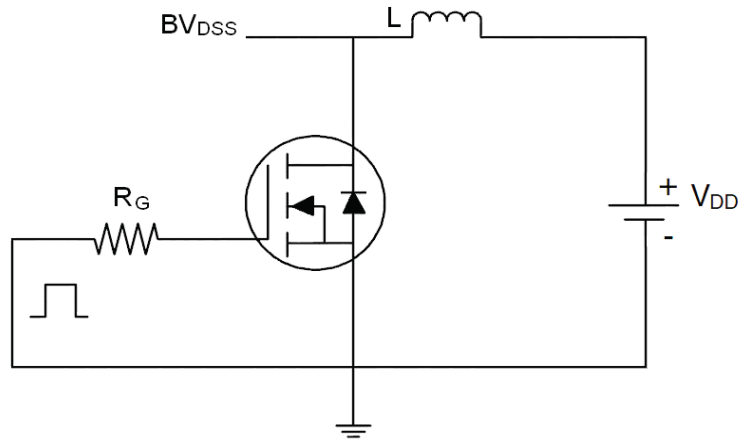
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	35	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	1.9	2.5	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$		2.9	3.5	
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	32	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	5000	-	PF
Output Capacitance	$C_{oss}$		-	1135	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	563	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	26	-	nS
Turn-on Rise Time	$t_r$		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	91	-	nS
Turn-Off Fall Time	$t_f$		-	39	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=20A,$ $V_{GS}=10V$	-	38		nC
Gate-Source Charge	$Q_{gs}$		-	9		nC
Gate-Drain Charge	$Q_{gd}$		-	13		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	100	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	42	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	39	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

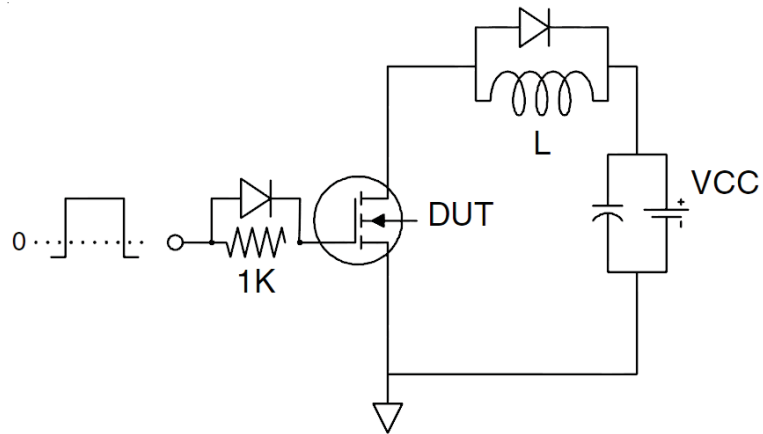
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

**Test circuit**

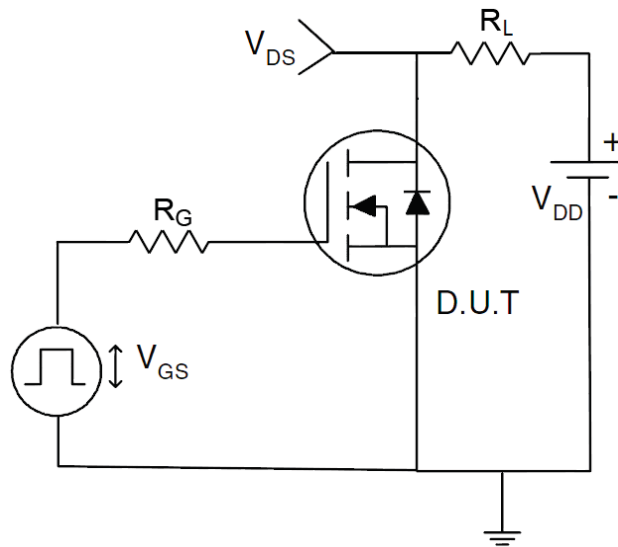
**1)  $E_{AS}$  Test Circuit**



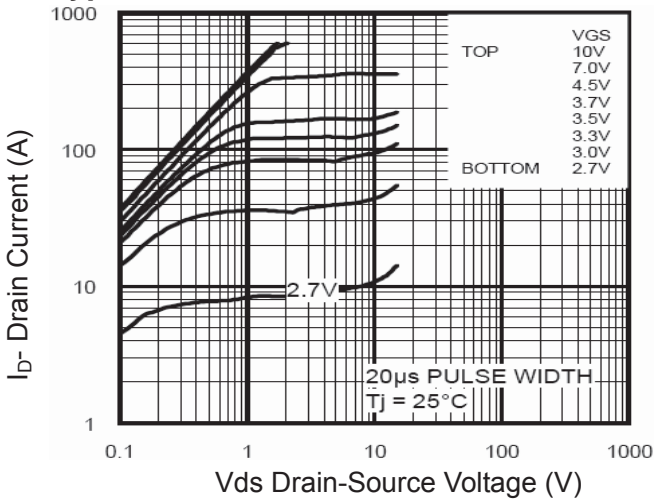
**2) Gate Charge Test Circuit**



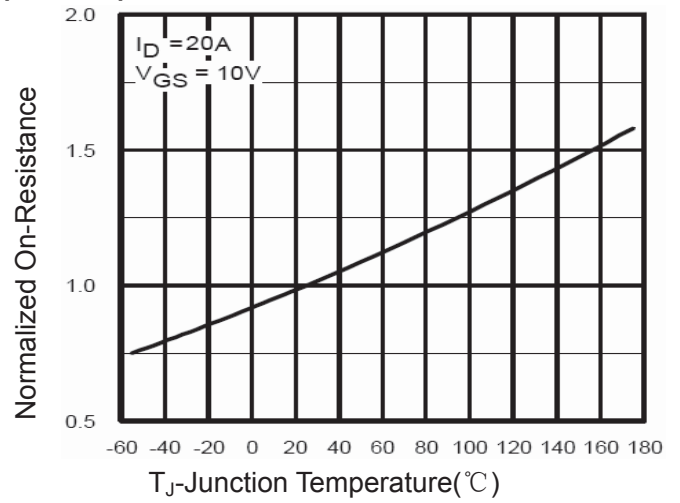
**3) Switch Time Test Circuit**



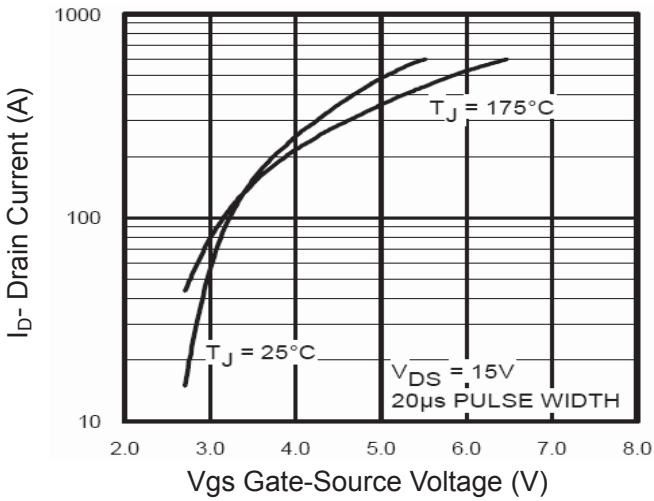
**Typical Electrical and Thermal Characteristics (Curves)**



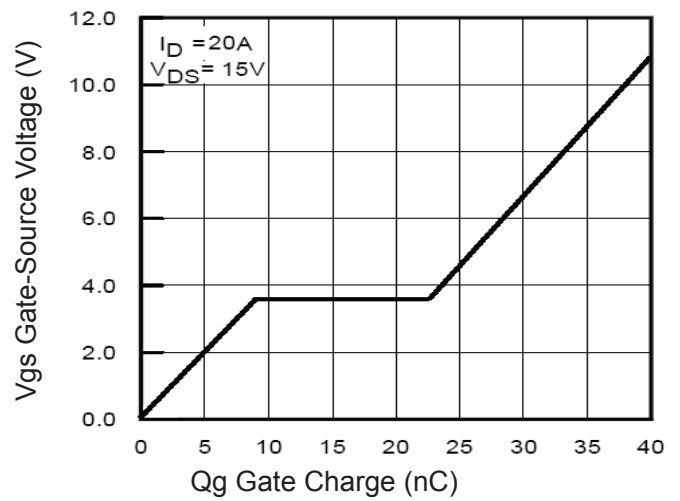
**Figure 1 Output Characteristics**



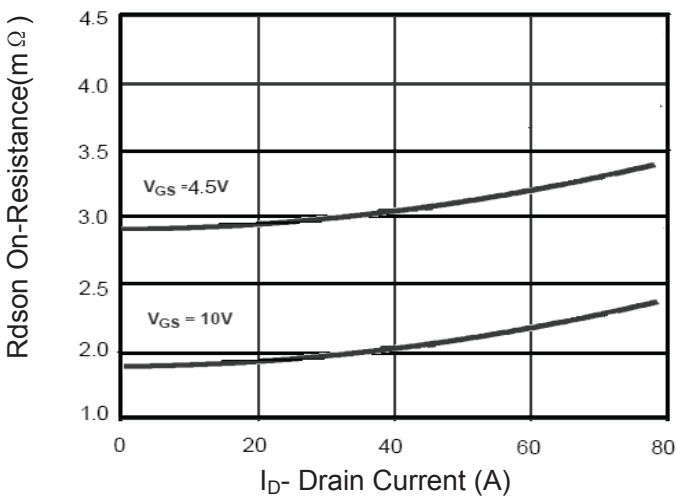
**Figure 4 Rdson-Junction Temperature**



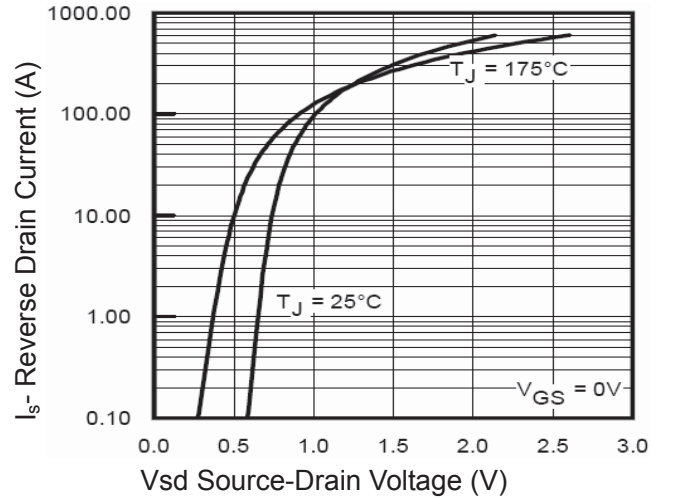
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**



**Figure 3 Rdson- Drain Current**



**Figure 6 Source- Drain Diode Forward**

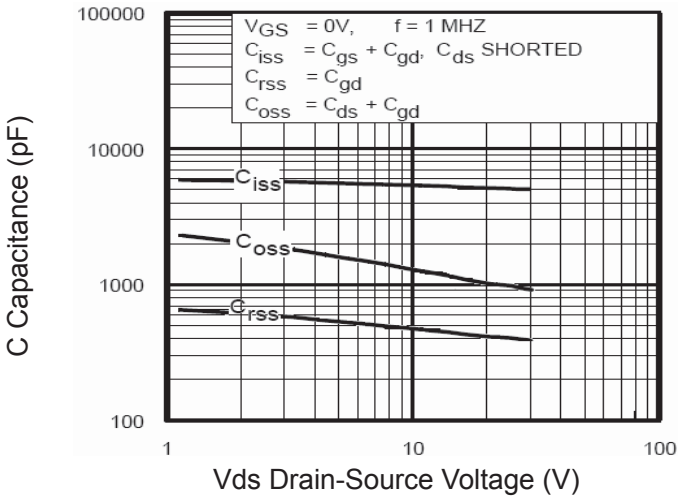


Figure 7 Capacitance vs Vds

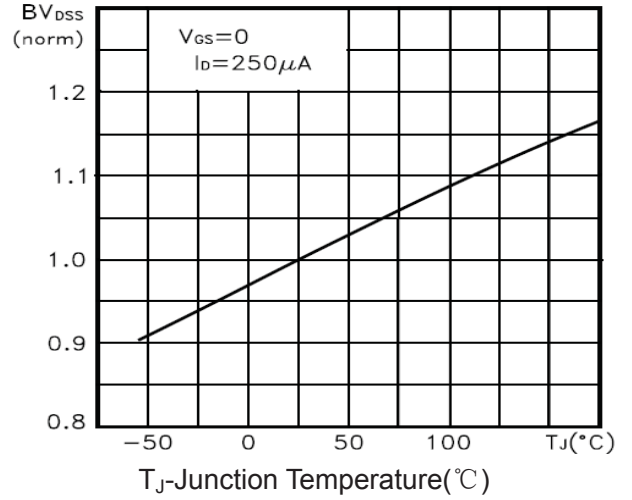


Figure 9  $BV_{DSS}$  vs Junction Temperature

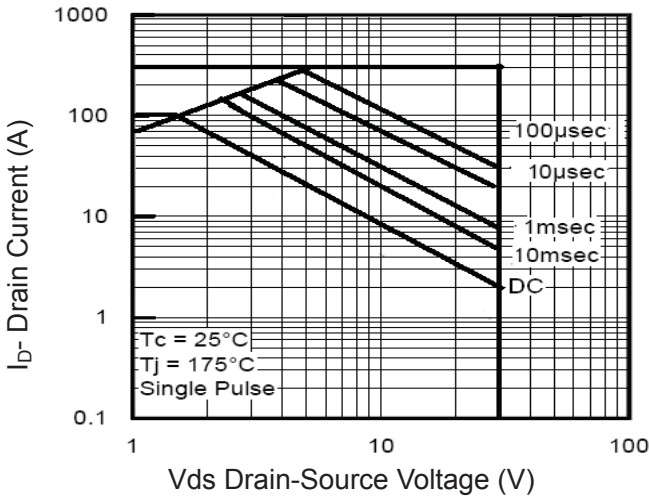


Figure 8 Safe Operation Area

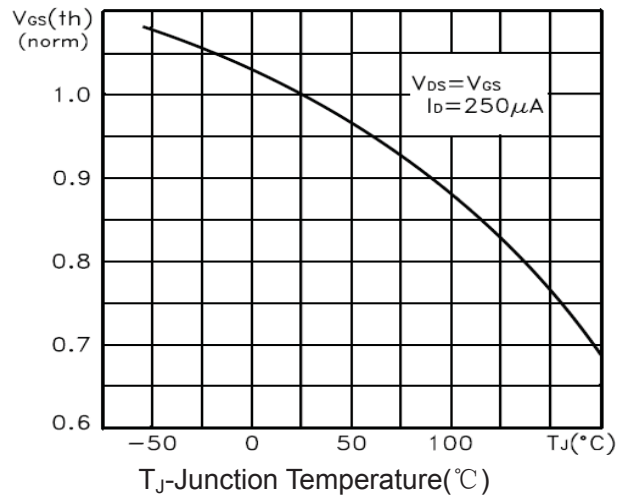


Figure 10  $V_{GS(th)}$  vs Junction Temperature

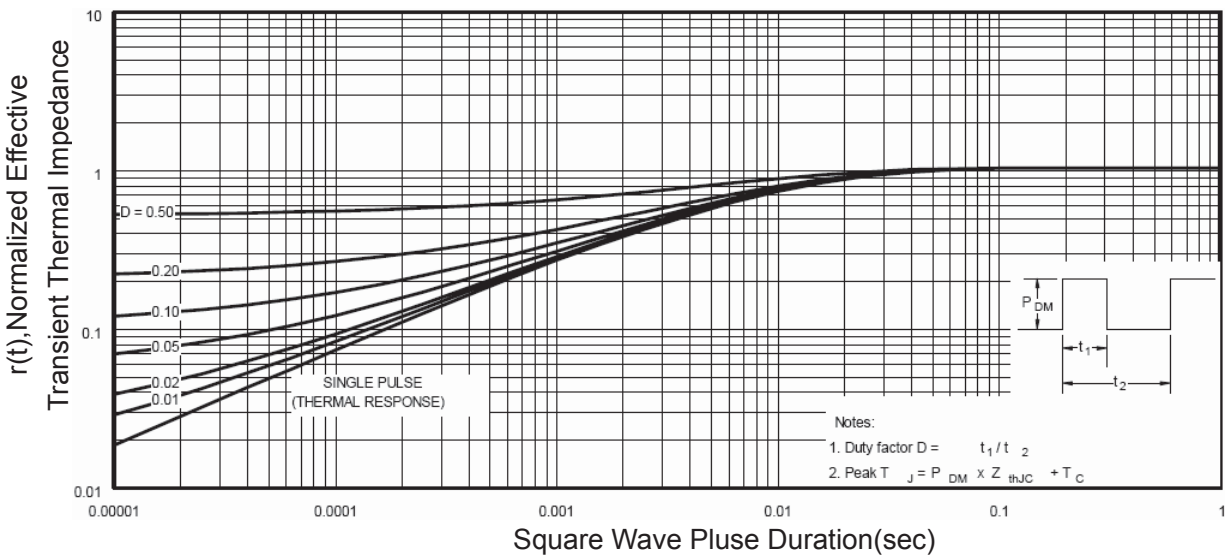
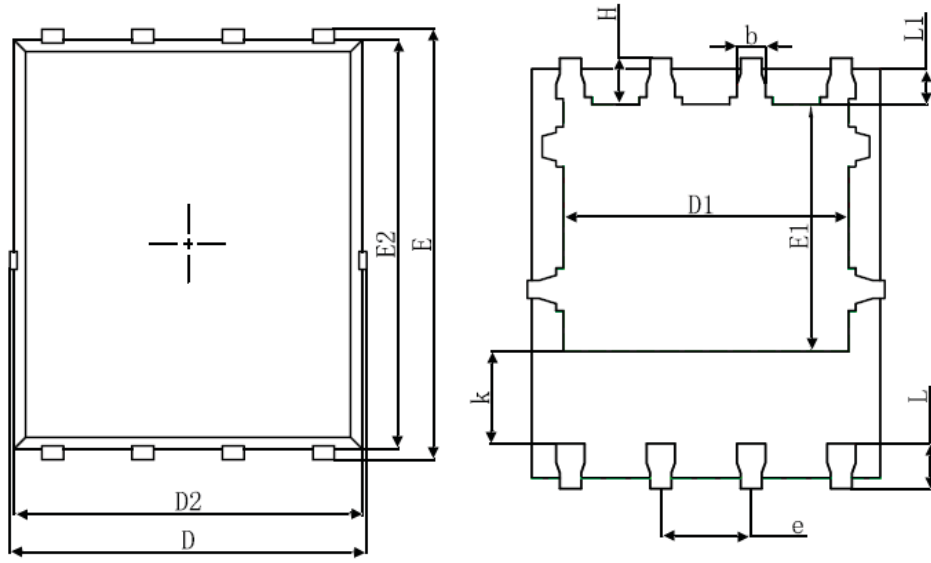


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Top View  
[顶视图]

Bottom View  
[背视图]

Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	8°	12°	8°	12°

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