

MT8362N3

Dual N & P-Channel PowerTrench[®] MOSFET

General Description

These dual N and P-Channel enhancement mode power field effect transistors are produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

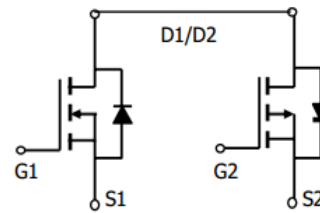
- N-Channel
30V/10A
 $R_{DS(on)} = 0.021\Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 0.033\Omega @ V_{GS} = 4.5V$
- P-Channel
-30V/-6A
 $R_{DS(on)} = 0.050\Omega @ V_{GS} = -10V$
 $R_{DS(on)} = 0.075\Omega @ V_{GS} = -4.5V$



MT Semiconductor[®]

<http://www.mtsemi.com>

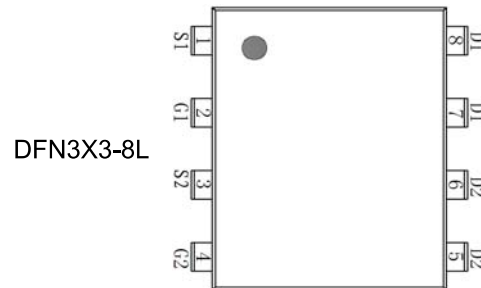
Simplified Schematic



N-channel

P-channel

MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-CH	P-CH	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a) - Pulsed	10	-6	A
		30	-18	
P_D	Power Dissipation for Dual Operation	3.5		W
	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.6		
		1.5		
		1.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	68	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	35	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT8362N3	MT8362N3	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	N-CH P-CH	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-CH P-CH		25 -22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	N-CH P-CH			1 -1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	N-CH P-CH	1 -1	1.6 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	N-CH P-CH		-4.3 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	N-CH		21 30 33	25 35 38	m Ω
		$V_{GS} = -10\text{ V}, I_D = -8\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -8\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -6\text{ A}$	P-CH		50 58 75	54 78 80	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	N-CH P-CH	10 -6			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -5\text{ A}$	N-CH P-CH		19 11		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-CH P-CH		809 690		pF
C_{oss}	Output Capacitance		P-CH		163 306		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-CH P-CH		68 77		pF

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

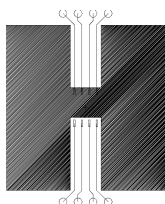
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	N-CH $V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	N-CH		2.2	4.4	ns
			P-CH		6.7	13.4	
t_r	Turn-On Rise Time		N-CH		7.5	15	ns
			P-CH		9.7	19.4	
$t_{d(off)}$	Turn-Off Delay Time	P-CH $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	N-CH		11.8	21.3	ns
			P-CH		19.8	35.6	
t_f	Turn-Off Fall Time		N-CH		3.7	7.4	ns
			P-CH		12.3	22.2	
Q_g	Total Gate Charge	N-CH $V_{DS} = 15\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}$	N-CH		18	26	nC
			P-CH		14	23	
Q_{gs}	Gate-Source Charge	P-CH $V_{DS} = -15\text{ V}, I_D = -5\text{ A}, V_{GS} = -10\text{ V}$	N-CH		2.5		nC
			P-CH		2.4		
Q_{gd}	Gate-Drain Charge		N-CH		2.6		nC
			P-CH		4.8		

Drain-Source Diode Characteristics and Maximum Ratings

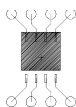
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-CH			10	A
			P-CH			-6	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	N-CH		0.81	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	P-CH		-0.85	-1.2	

Notes:

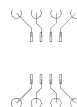
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°W/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°W/W when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) 135°W/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics: N-CH

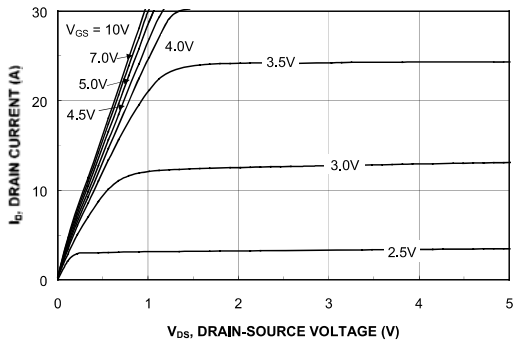


Figure 1. On-Region Characteristics.

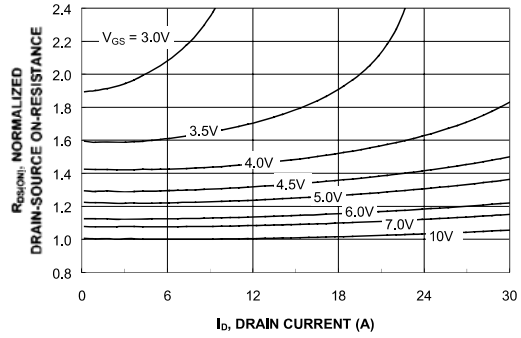


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

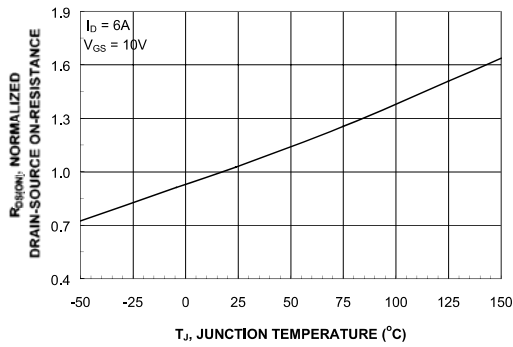


Figure 3. On-Resistance Variation with Temperature.

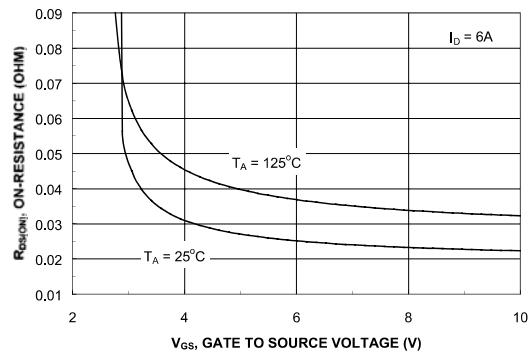


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

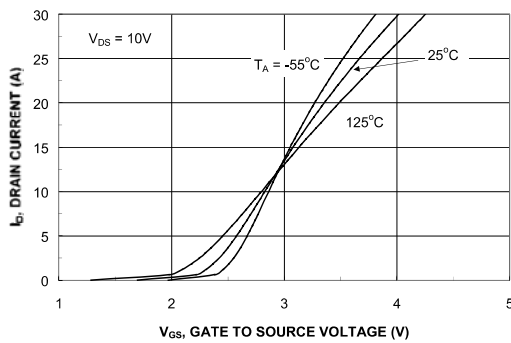


Figure 5. Transfer Characteristics.

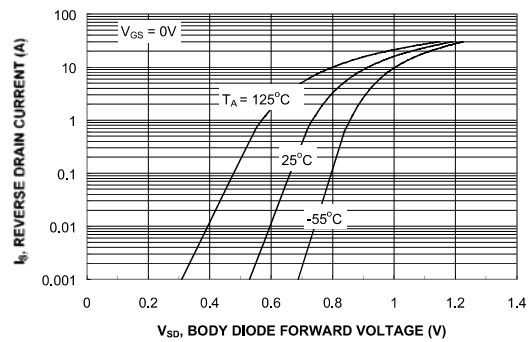


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-CH

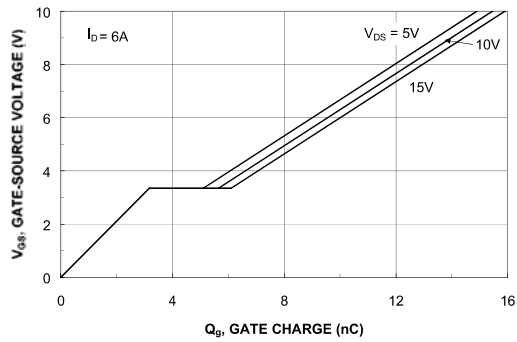


Figure 7. Gate Charge Characteristics.

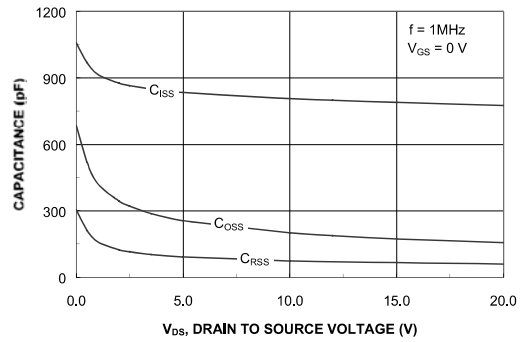


Figure 8. Capacitance Characteristics.

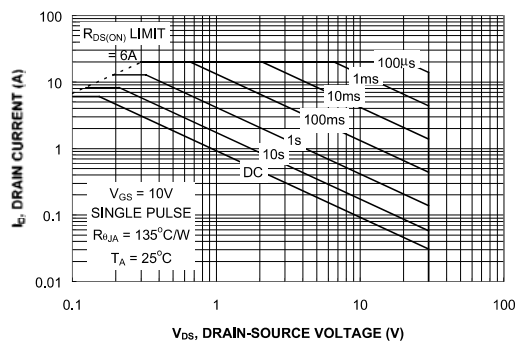


Figure 9. Maximum Safe Operating Area.

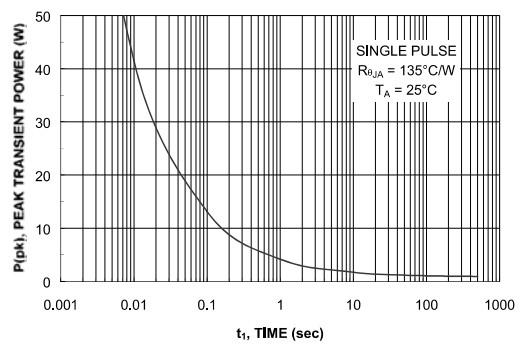


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics P-CH

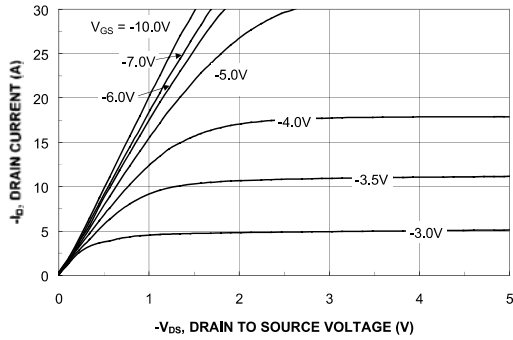


Figure 11. On-Region Characteristics.

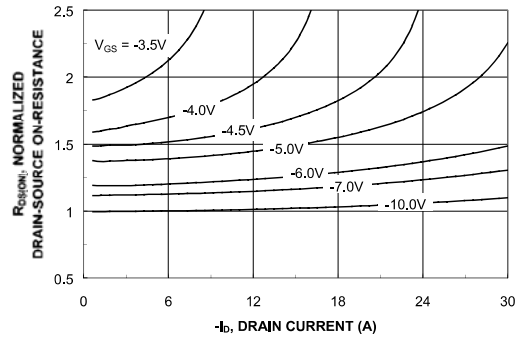


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

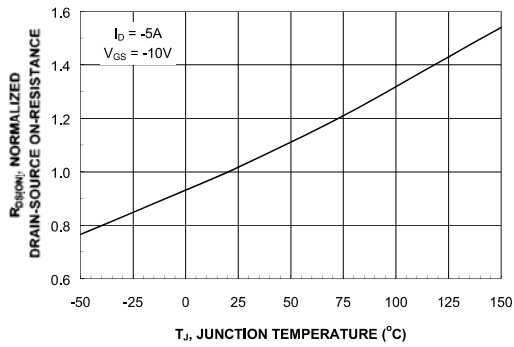


Figure 13. On-Resistance Variation with Temperature.

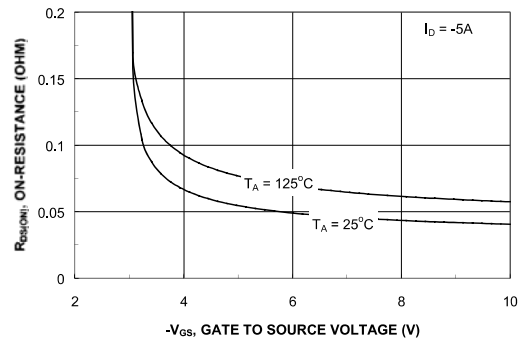


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

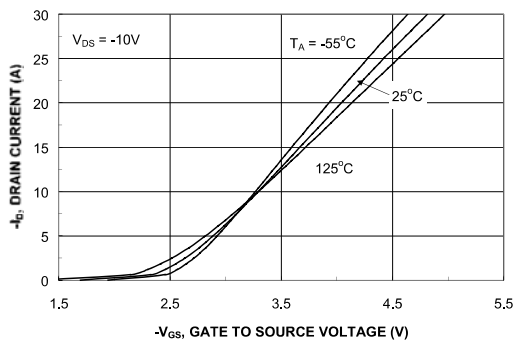


Figure 15. Transfer Characteristics.

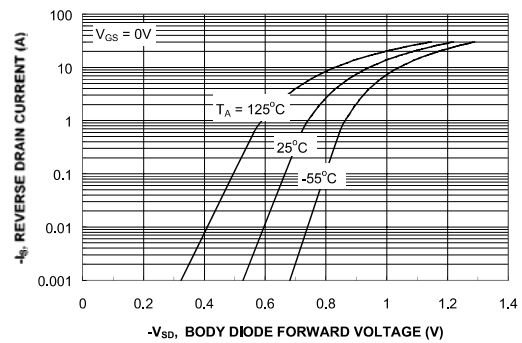


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics P-CH

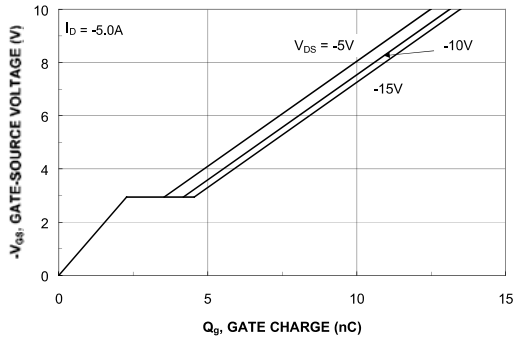


Figure 17. Gate Charge Characteristics.

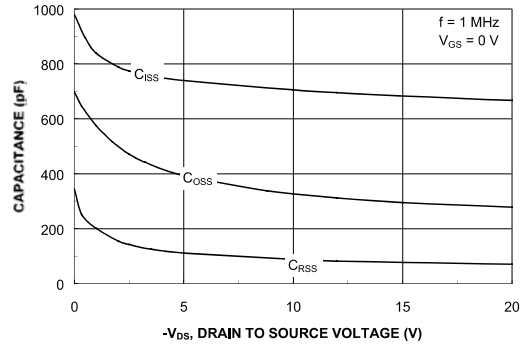


Figure 18. Capacitance Characteristics.

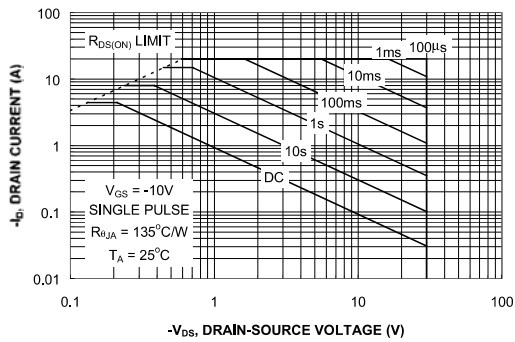


Figure 19. Maximum Safe Operating Area.

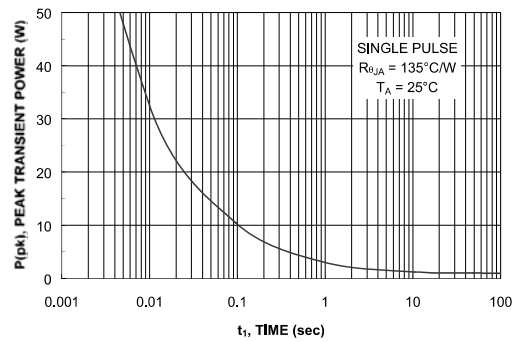


Figure 20. Single Pulse Maximum Power Dissipation.

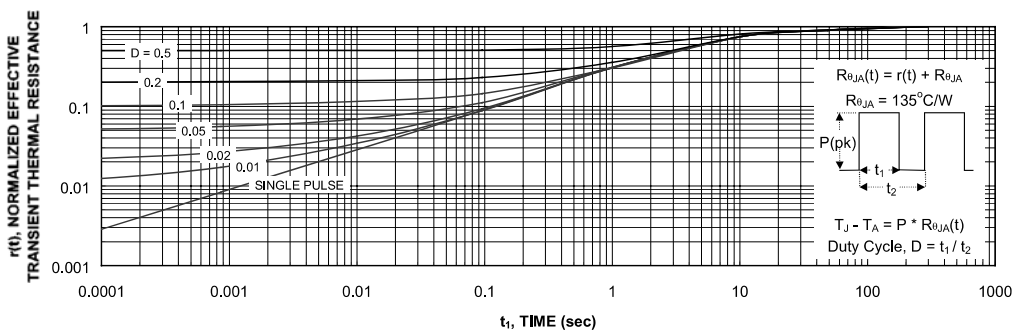
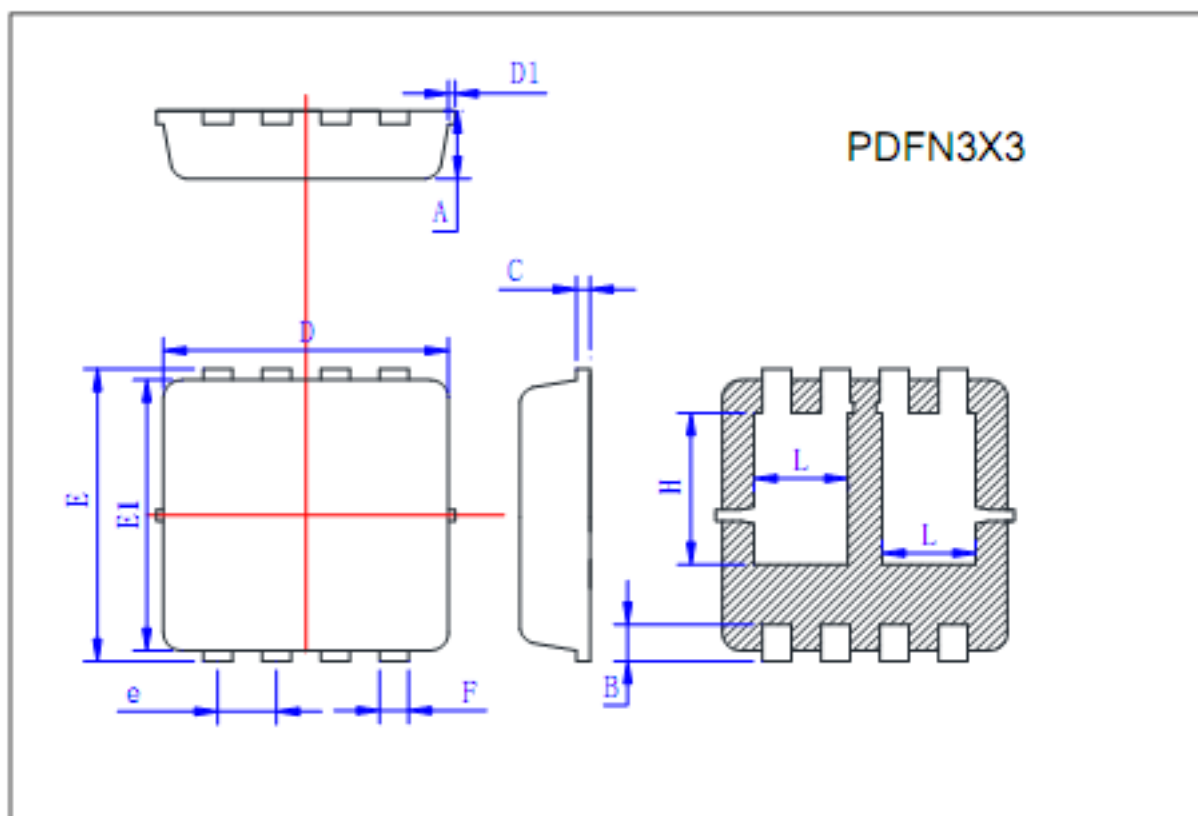


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

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10. 本公司一直致力于提高产品的质量和可靠性, 但一般来说, 半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失, 希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等, 这是作为机器和系统的出厂保证。特别是单片机的软件, 由于单独进行验证很困难, 所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
11. 如果把本资料所记载的产品从其载体设备上卸下, 有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时, 请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时, 本公司将不承担任何责任。
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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.