

MT83N05N5

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = 30V$
- $I_D = 80A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} = 4.5m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} = 8.0m\Omega$ @ $V_{GS} = 4.5V$

Features

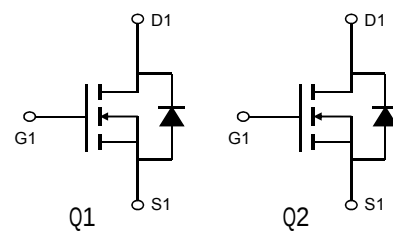
- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.
- PDFN5x6-8L Package



MT Semiconductor®

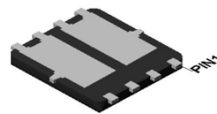
<http://www.mtsemi.com>

Simplified Schematic

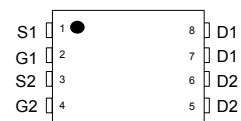


MARKING DIAGRAM & PIN ASSIGNMENT

DFN5X6-8L



Top View



Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter		Steady State	Units
V _{DS}	Drain-Source Voltage		30	V
V _{GS}	Gate-Source Voltage		±20	V
I _D	Continuous Drain Current ¹	T _C = 25°C	80	A
I _{DM}	Pulsed Drain Current ²		260	A
I _S	Continuous Source Current (Diode Conduction) ¹		60	A
E _{AS}	Single Pulse Drain-Source Avalanche Energy ³		110	mJ
P _D	Maximum Power Dissipation	T _A = 25°C	2	W
		T _C = 25°C	80	
T _J , T _{STG}	Operating Junction and Storage Temperature Range		-55~150	°C

Notes:

1. Surface Mounted on 1" x 1" FR4 Board, $t \leq 10$ Sec.
2. Pulse width limited by maximum junction temperature.
3. The test condition is $T_J = 25^\circ C$, $V_{DD} = 30V$, $V_{GS} = 10V$, $L = 0.1mH$, $R_G = 25\Omega$, $I_{AS} = 50A$.

Thermal Resistance Ratings

Symbol	Parameter	Typical	Maximum	Unit
R _{thJA}	Maximum Junction-to-Ambient	-	62.5	°C/W
R _{thJC}	Maximum Junction-to-Case	-	1.4	

Electrical Characteristics (T_A=25°C, unless otherwise noted)

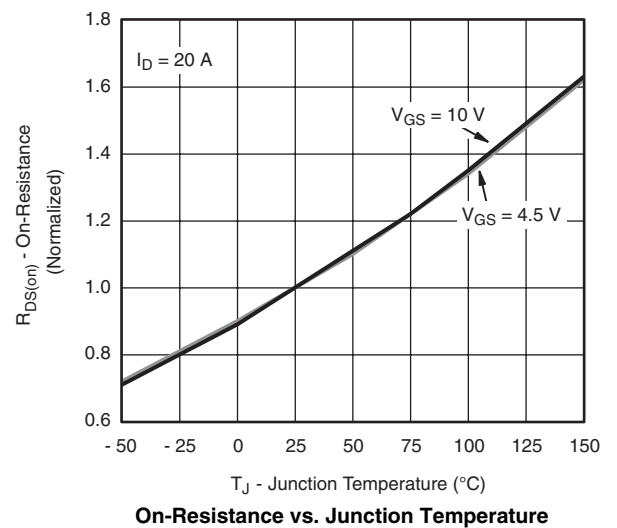
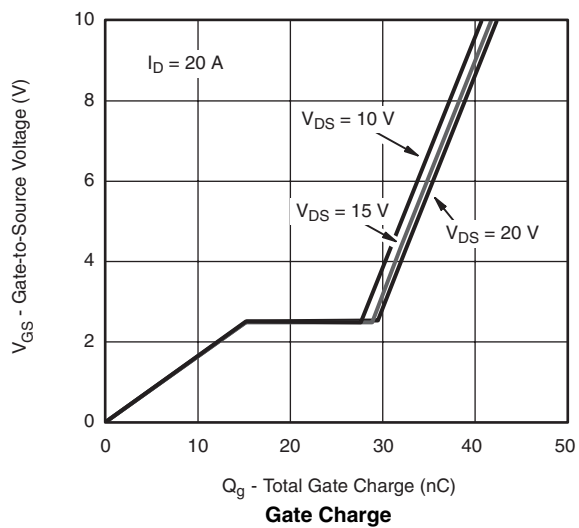
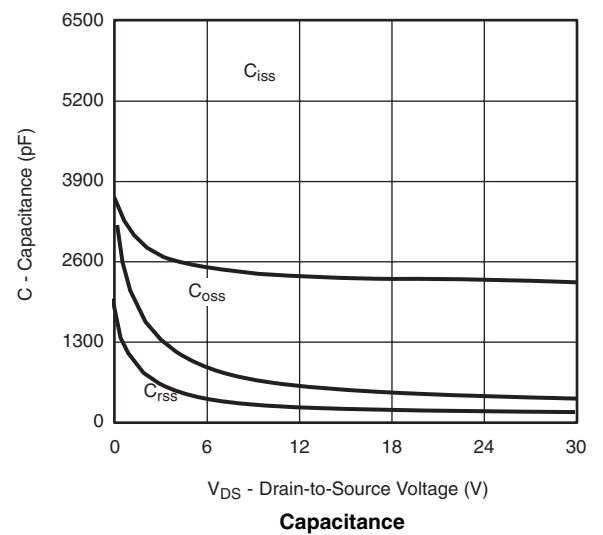
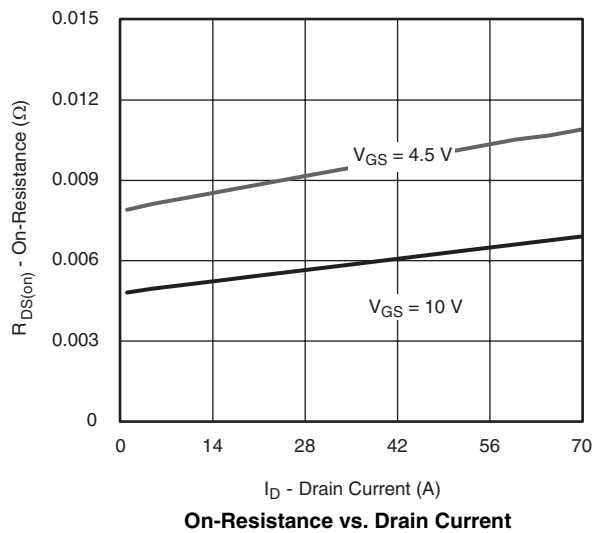
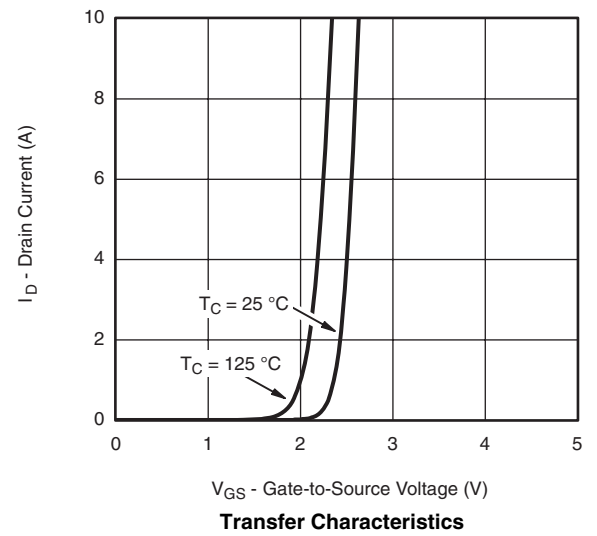
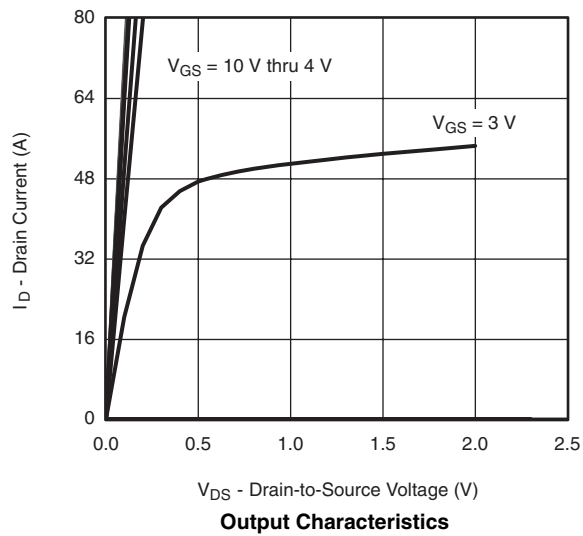
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	1.0	1.5	2.0	V
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24V, V _{GS} = 0V	-		1	μA
		V _{DS} = 24V, V _{GS} = 0V, T _J = 85°C	-		30	
R _{DS(on)}	Drain Source On State Resistance ^a	V _{GS} = 10V, I _D = 20A	-	4.5	5.5	mΩ
		V _{GS} = 4.5V, I _D = 10A	-	8.0	11	
V _{SD}	Diode Forward Voltage ^a	V _{GS} = 0V, I _S = 20A	-	0.82	1.3	V
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz	-	1850	-	pF
C _{oss}	Output Capacitance		-	465	-	
C _{rss}	Reverse Transfer Capacitance		-	260	-	
Q _g	Total Gate Charge	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A	-	41	-	nC
Q _{gs}	Gate-Source Charge		-	15	-	
Q _{gd}	Gate-Drain Charge		-	12	-	
t _{d(on)}	Turn-On Delay Time	V _{DD} = 15V, V _{GS} = 10V I _D = 20A, R _{GEN} = 3Ω	-	22	-	nSec
t _r	Rise Time		-	35	-	
t _{d(off)}	Turn-Off Delay Time		-	50	-	
t _f	Fall Time		-	27	-	
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt= 100A/μA, T _J =25°C	-	33	-	nSec

Note:

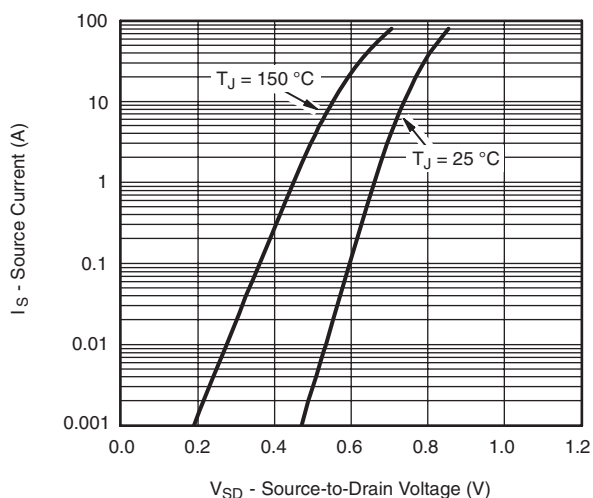
a. Pulse test; pulse width ≤300μs, duty cycle ≤2%.

b. Guaranteed by design, not subject to production testing.

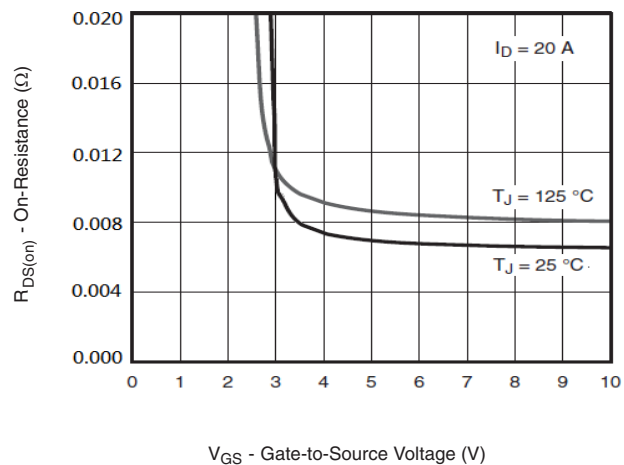
Characteristics Curve



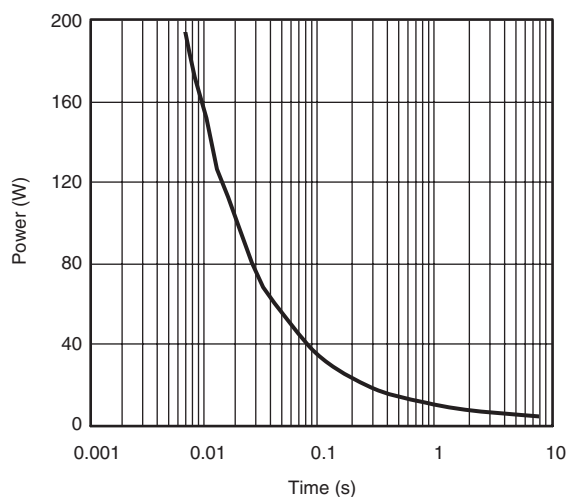
Characteristics Curve



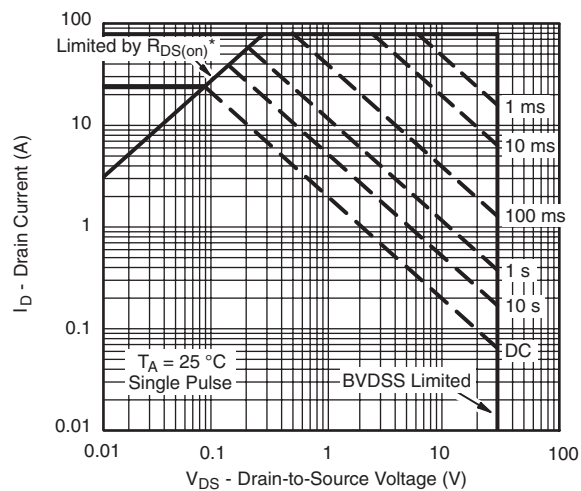
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

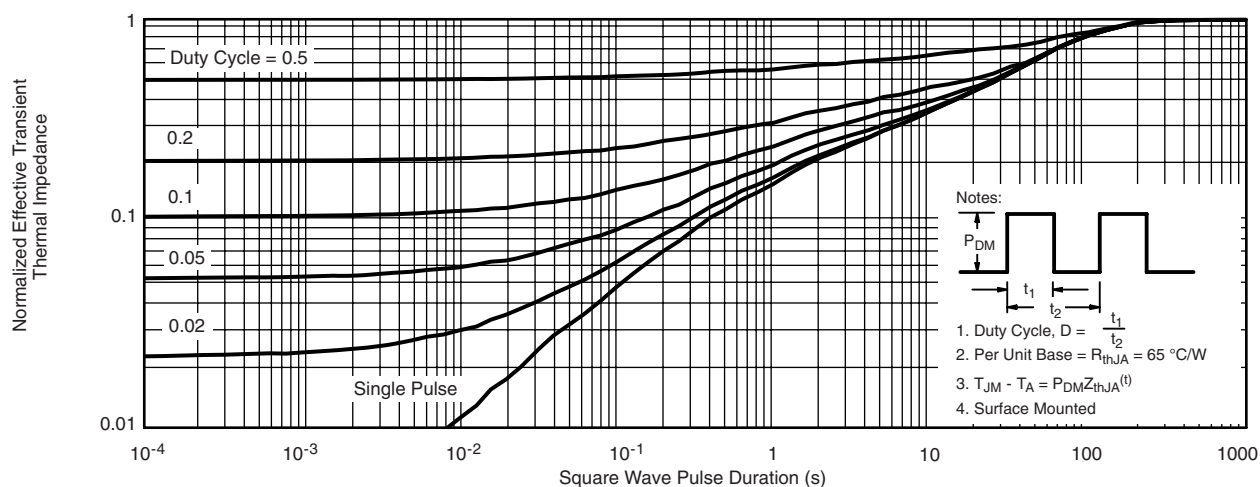


Single Pulse Power, Junction-to-Ambient



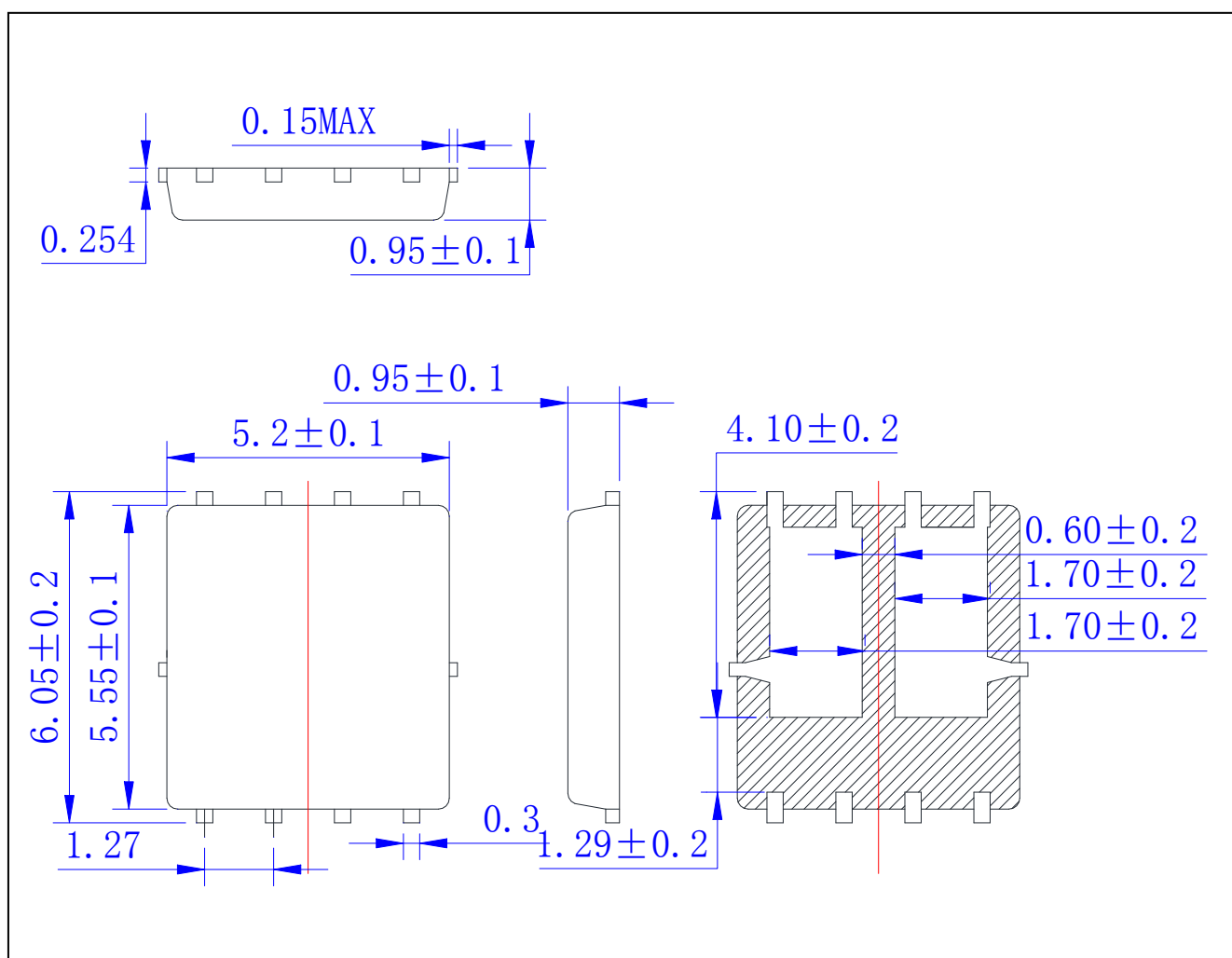
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

DFN5×6 OUTLINE



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