

# MT83P05N3

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS} = -30V$
- $I_D = -60A$
- $R_{DS(ON)} \leq 9m\Omega$  @  $V_{GS} = -10V$
- $R_{DS(ON)} \leq 15.0m\Omega$  @  $V_{GS} = -4.5V$

### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

### Applications

- Notebook Computer
- Portable Battery Pack

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	10s	Steady State	Units
$V_{DS}$	Drain-Source Voltage		-30	V
$V_{GS}$	Gate-Source Voltage		$\pm 20$	V
$I_D$	Continuous Drain Current <sup>1</sup>	-55	-60	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>		-50	A
$I_S$	Continuous Source Current (Diode Conduction) <sup>1</sup>	-2.7	-1.36	A
$P_D$	Maximum Power Dissipation <sup>1</sup>	5.0	2.5	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range		-55 to 150	°C

### Thermal Resistance Ratings

Symbol	Parameter	Typical	Maximum	Unit
$R_{thJA}$	Maximum Junction-to-Ambient <sup>1</sup>	$t \leq 10$ Sec	33	42
		Steady State	70	82

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

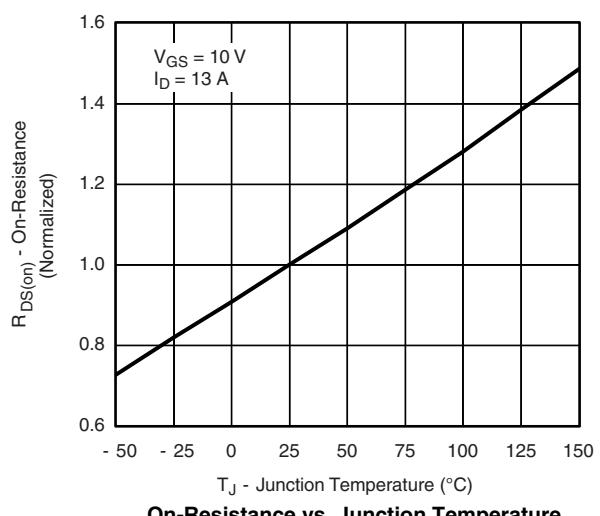
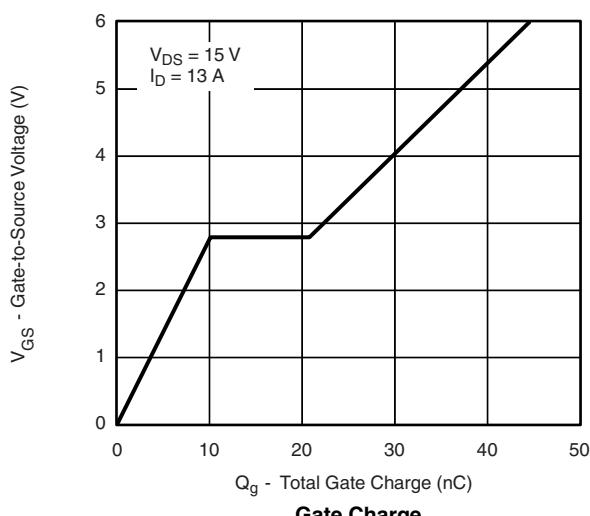
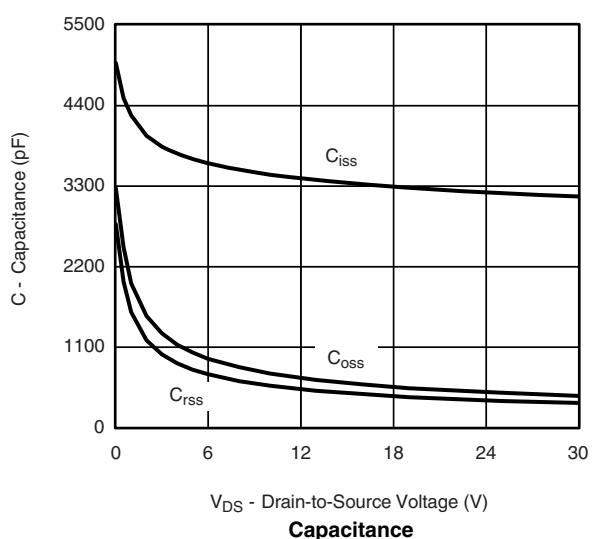
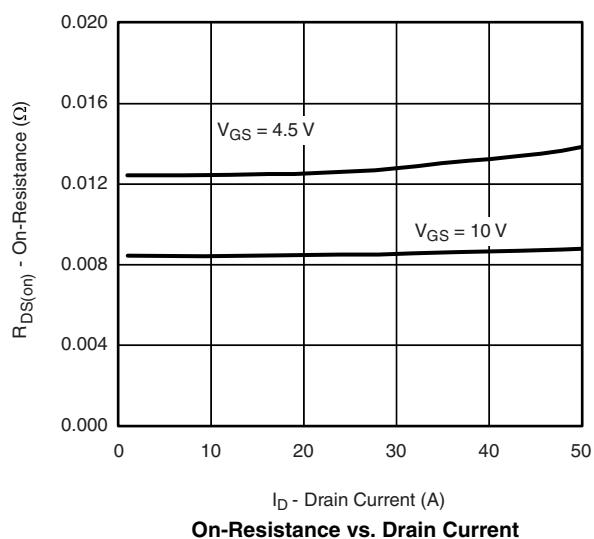
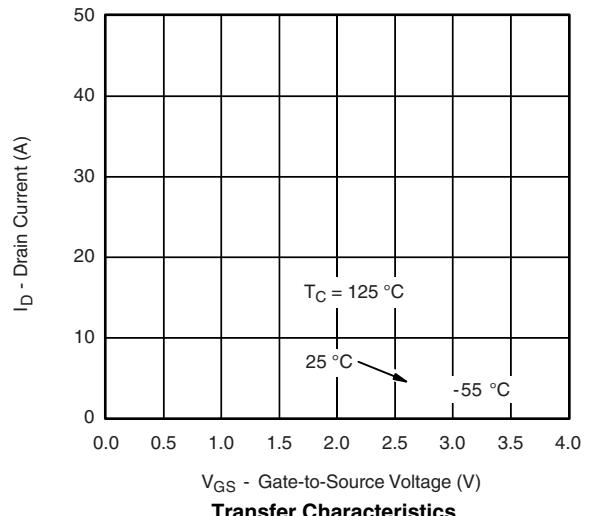
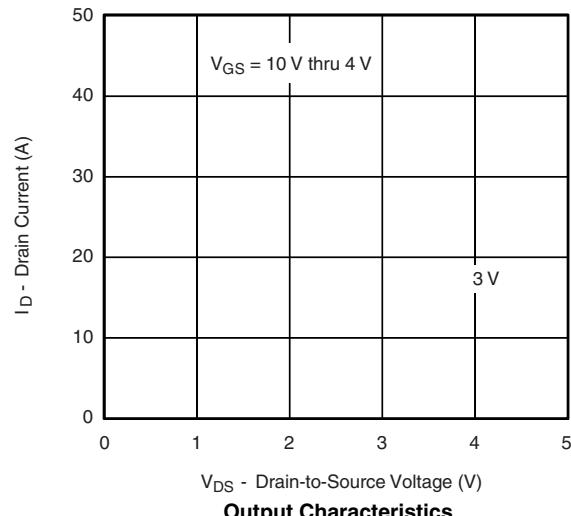
## Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>• Static Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-1.0	-1.6	-3	V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	-	-	±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	-	-	-1	μA
		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 70°C		-	-10	
R <sub>DSS(on)</sub>	Drain Source On State Resistance <sup>a</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -12A	-	6.5	9	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -8A	-	9.3	15	
g <sub>fs</sub>	Forward Transconductance <sup>a</sup>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -9A	-	40	-	S
V <sub>SD</sub>	Diode Forward Voltage <sup>a</sup>	I <sub>S</sub> = -2.7A, V <sub>GS</sub> = 0V	-	-0.74	-1.1	V
<b>• Dynamic Characteristics <sup>b</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz	-	3540.0	-	pF
C <sub>oss</sub>	Output Capacitance		-	577.0	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	426.0	-	
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -5V, I <sub>D</sub> = -13A	-	47.0	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	10.0	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	11.0	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -15V, R <sub>L</sub> = 15Ω I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 6Ω	-	19.5	-	nSec
t <sub>r</sub>	Rise Time		-	10.0	-	
T <sub>d(off)</sub>	Turn-Off Delay Time		-	137.5	-	
t <sub>f</sub>	Fall Time		-	55.3	-	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0, f = 1MHz	-	3.4	-	Ω
t <sub>rr</sub>	Source-Drain Reverse Recovery Time	I <sub>F</sub> = -2.1A, di/dt = 100A/μs	-	60	100	nSec

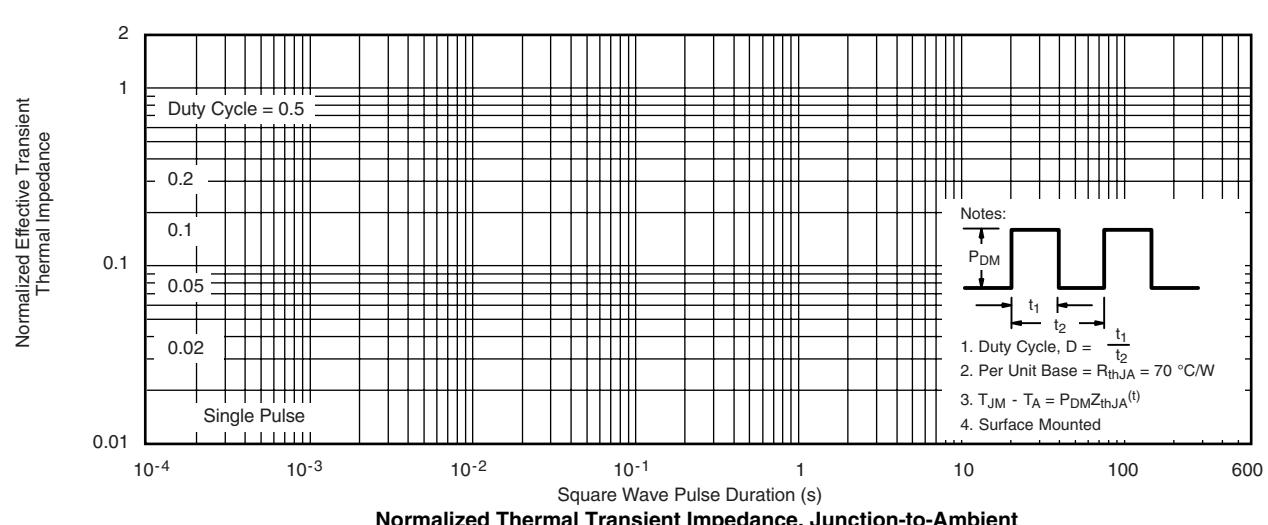
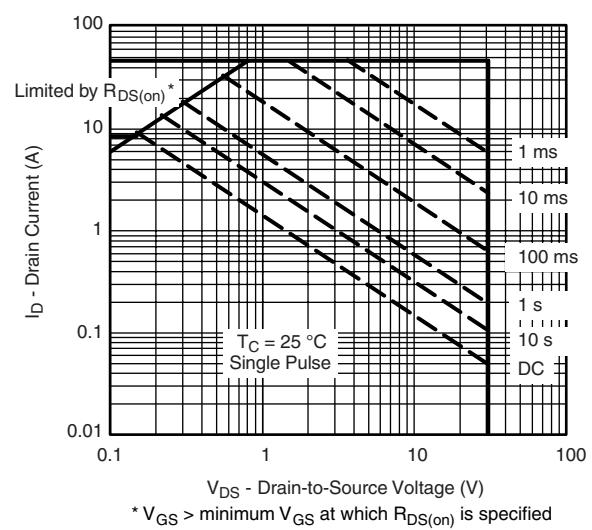
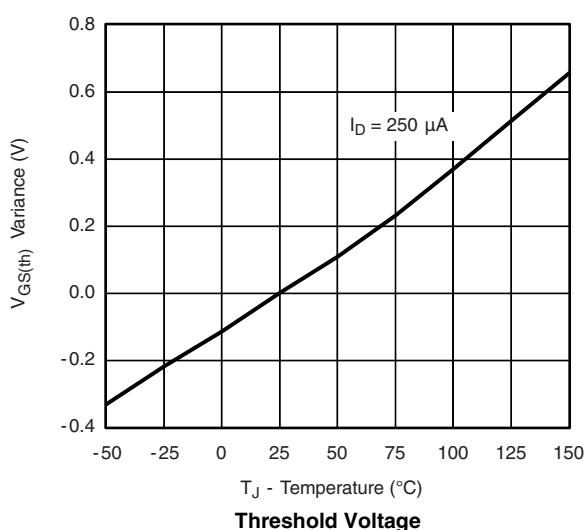
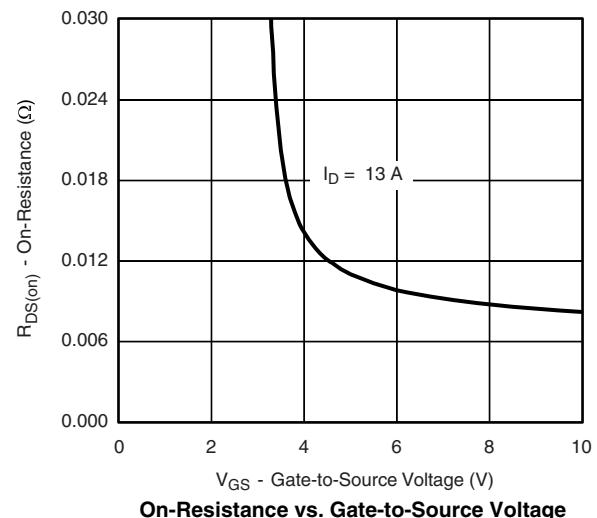
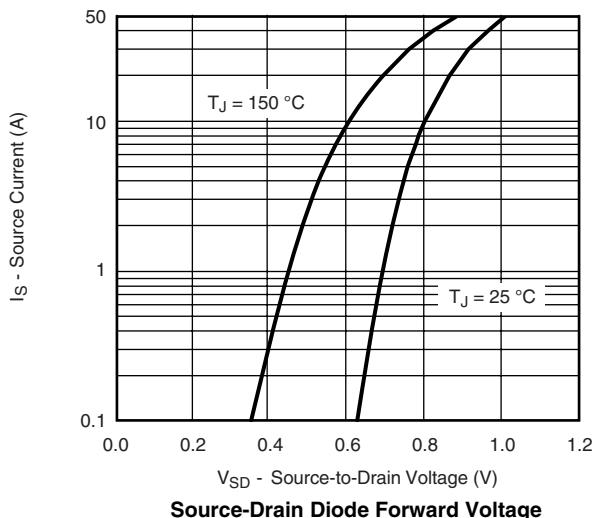
Note:

- a. Pulse test; pulse width  $\leq$  300μs, duty cycle  $\leq$  2%.
- b. Guaranteed by design, not subject to production testing.

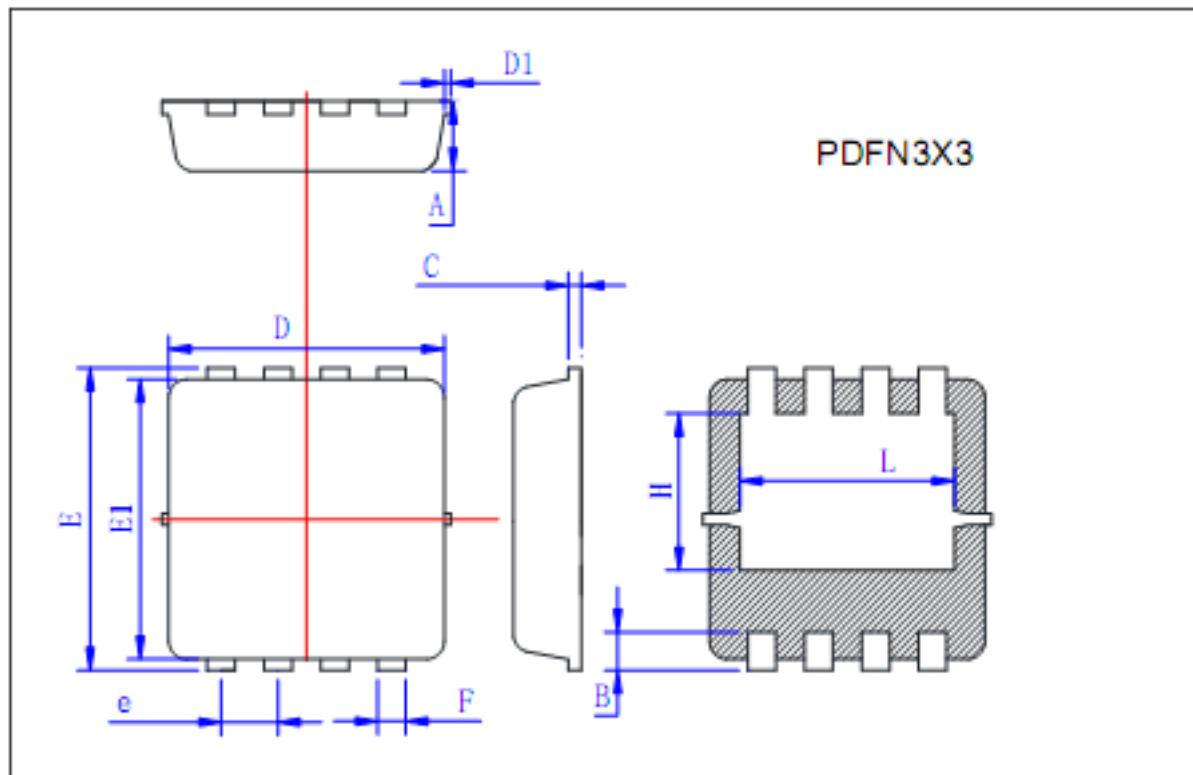
## Characteristics Curve ( $T_A=25^\circ\text{C}$ , unless otherwise noted)



## Characteristics Curve ( $T_A=25^\circ\text{C}$ , unless otherwise noted)



## PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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