

MT83P08N3

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = -30V$
- $I_D = -12A$
- $R_{DS(ON)} = 10m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} = 12m\Omega @ V_{GS} = -4.5V$

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

Applications

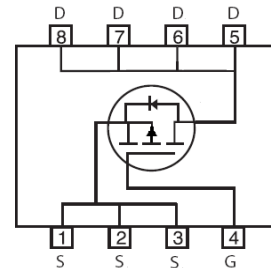
- Notebook Computer
- Portable Battery Pack



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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



DFN3X3-8L

PIN1

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	10s	Steady State	Units
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current ¹	-14	-12	A
I_{DM}	Pulsed Drain Current ²		-50	A
I_S	Continuous Source Current (Diode Conduction) ¹	-2.7	-1.36	A
P_D	Maximum Power Dissipation ¹	3.0	1.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55 to 150	$^\circ C$

Thermal Resistance Ratings

Symbol	Parameter	Typical	Maximum	Unit
R_{thJA}	Maximum Junction-to-Ambient ¹	$t \leq 10$ Sec	33	$^\circ C/W$
		Steady State	70	

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

Electrical Characteristics (T_A=25°C, unless otherwise noted)

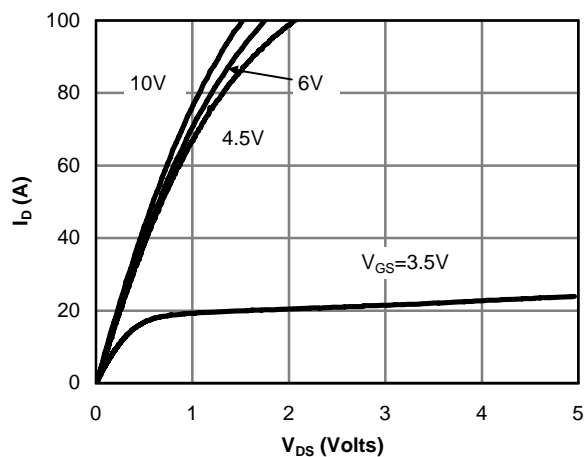
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
● Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = -250μA	-0.8	-	-1.5	V
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
		V _{DS} = -24V, V _{GS} = 0V, T _J = 70°C	-	-	-10	
R _{DS(on)}	Drain Source On State Resistance ^a	V _{GS} = -10V, I _D = -10A	-	10	12	mΩ
		V _{GS} = -4.5V, I _D = -8A	-	12	15	
g _{fs}	Forward Transconductance ^a	V _{DS} = -15V, I _D = -9A	-	40	-	S
V _{SD}	Diode Forward Voltage ^a	I _S = -2.7A, V _{GS} = 0V	-	-0.74	-1.1	V
● Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1MHz	-	3550.0	-	pF
C _{oss}	Output Capacitance		-	596.0	-	
C _{rss}	Reverse Transfer Capacitance		-	435.0	-	
Q _g	Total Gate Charge	V _{DS} = -15V, V _{GS} = -5V, I _D = -13A	-	39	-	nC
Q _{gs}	Gate-Source Charge		-	12	-	
Q _{gd}	Gate-Drain Charge		-	10	-	
t _{d(on)}	Turn-On Delay Time	V _{DD} = -15V, R _L = 15Ω I _D = -1A, V _{GEN} = -10V, R _G = 6Ω	-	19.5	-	nSec
t _r	Rise Time		-	10.0	-	
T _{d(off)}	Turn-Off Delay Time		-	137.5	-	
t _f	Fall Time		-	55.3	-	
R _g	Gate Resistance	V _{GS} = 0, V _{DS} = 0, f = 1MHz	-	3.4	-	Ω
t _{rr}	Source-Drain Reverse Recovery Time	I _F = -2.1A, di/dt = 100A/μs	-	60	100	nSec

Note:

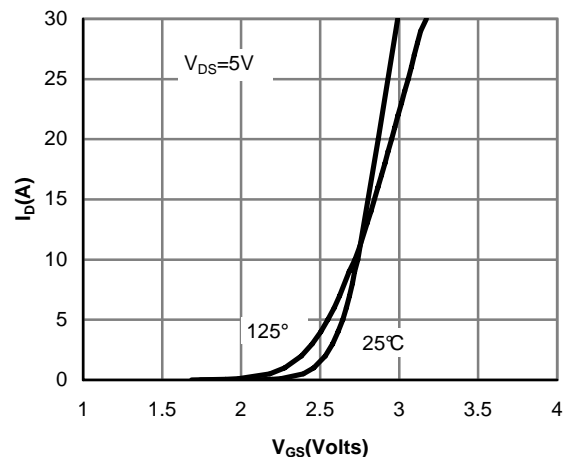
a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

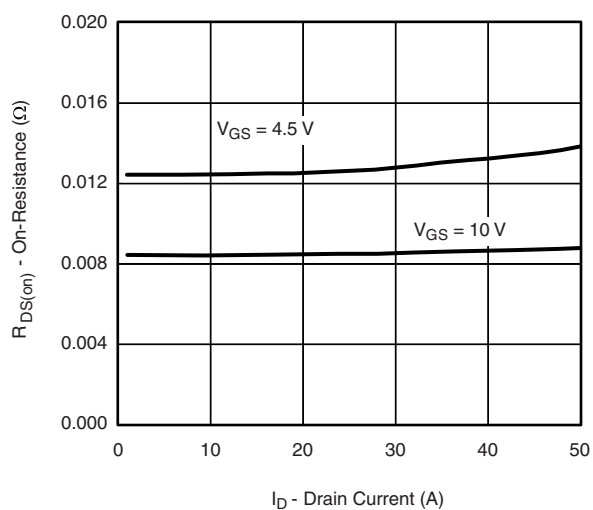
Characteristics Curve ($T_A=25^\circ\text{C}$, unless otherwise noted)



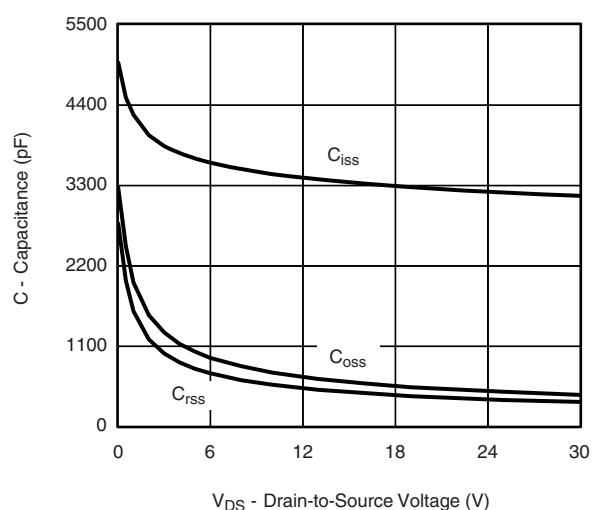
Output Characteristics



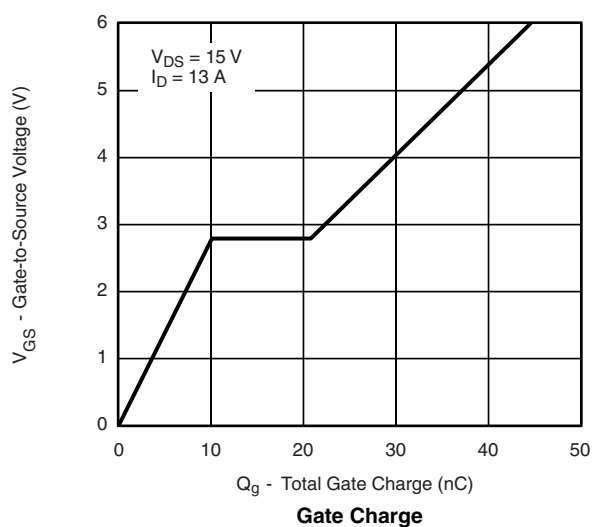
Transfer Characteristics



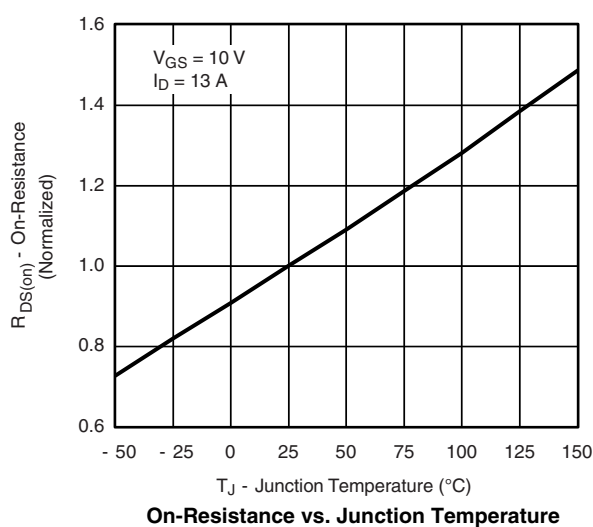
On-Resistance vs. Drain Current



Capacitance

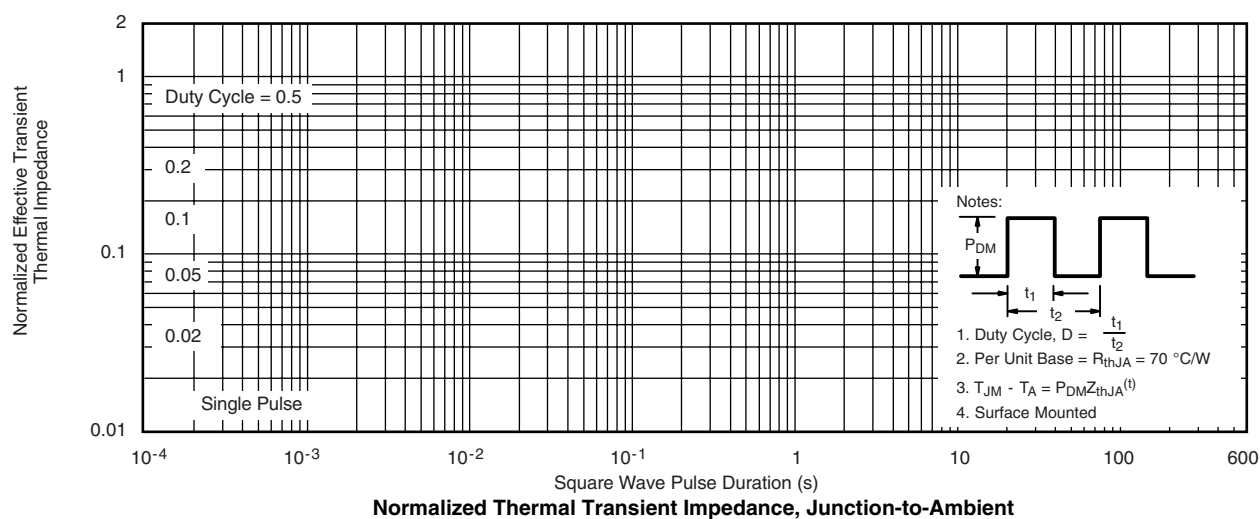
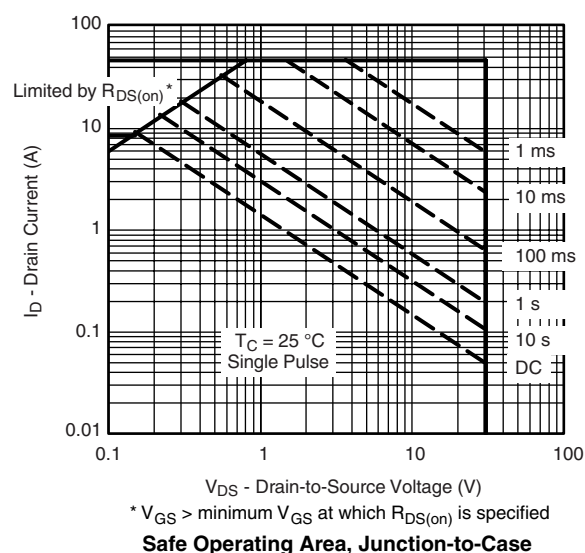
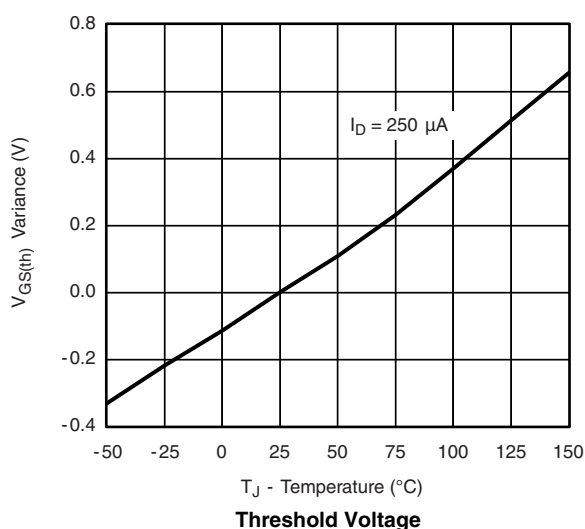
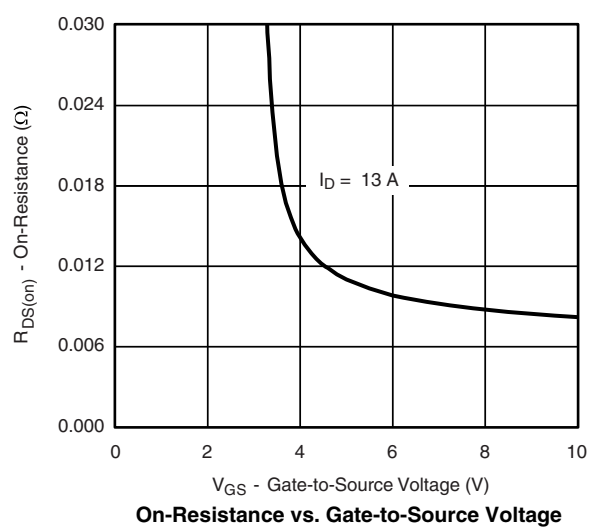
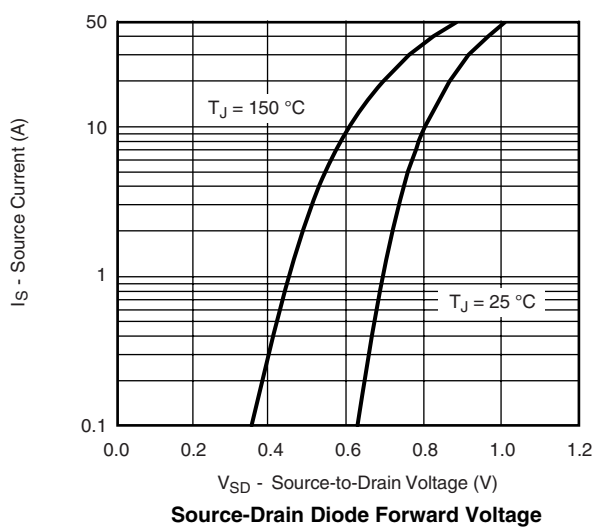


Gate Charge

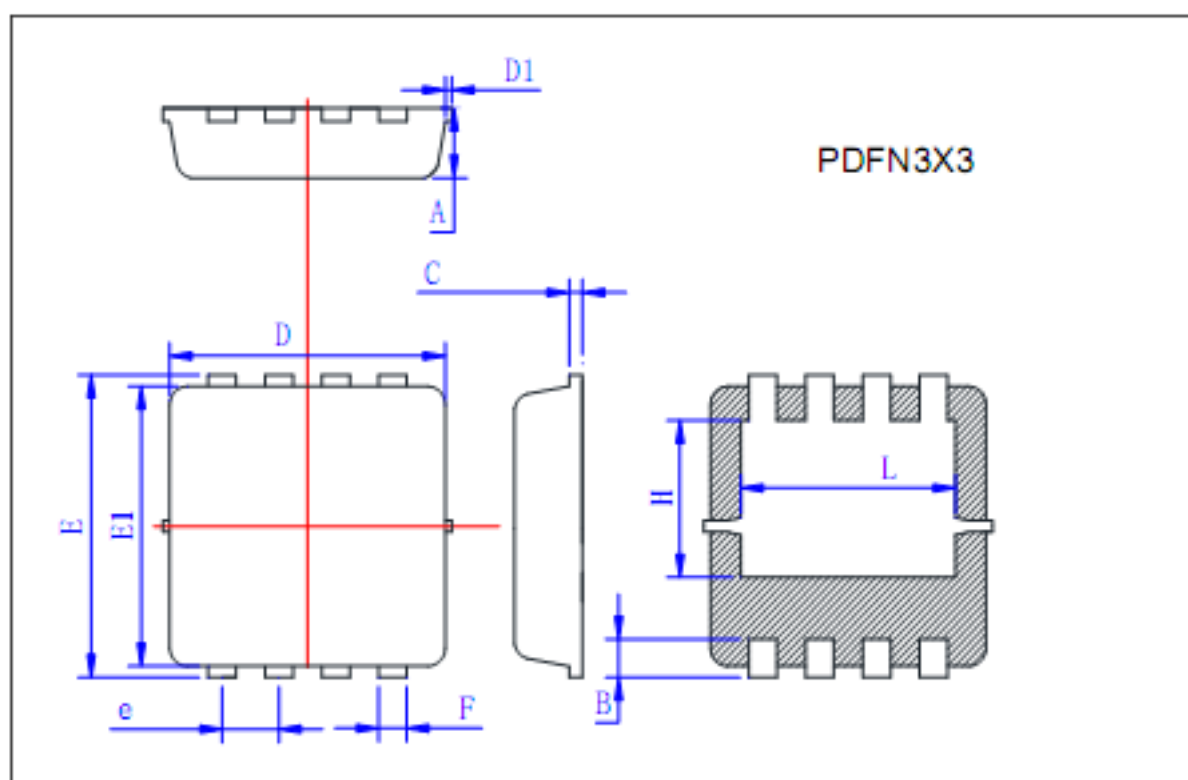


On-Resistance vs. Junction Temperature

Characteristics Curve ($T_A=25^\circ\text{C}$, unless otherwise noted)



PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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