MT9435A

P-Channel Enhancement Mode Field Effect Transistor

Product summary

PRODUCT SUMMARY								
V _{DSS}	ΙD	$Rds(ON)$ $(m \Omega)$ Typ						
-30V	561	45@ VGS=-10V						
	-5.6A	75 @ VGS=-4.5V						

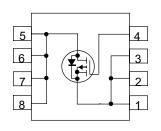
Features

- Supper high dense cell design for low RDS(ON)
- · Rugged and reliable
- · Sample drive requirment
- SOP-8 package



http://www.mtsemi.com

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Absolute Maximum Ratings(T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	Vds	-30	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous ^a @Tj=125 ℃	ID	-5.6	A
- Pulse d^b	Ідм	-24	A
Drain-source Diode Forward Current ^a	Is	-1.7	A
Maximum Power Dissipation ^a	PD	2.5	W
Operating Junction and Storage Temperature Range	TJ,Tstg	-55 to 150	${\mathbb C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to Ambient ^a Rth JA 50 °C/W

ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Uni
OFF CHARACTERISTICS				I		
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V,I _D =-250µA	-30			V
Zero Gate Voltage Drain Current	IDSS	V _{DS} =-24V,V _{GS} =0V			-1	μД
Gate-Body Leakage	Igss	$V_{GS}=\pm20V, V_{DS}=0V$			±100	nA
ON CHARACTERITICS						
Gate Threshold Voltage	V _G s(th)	V _{DS} =V _{GS} ,I _D =-250μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	Prayora	V _{GS} =-10V,I _D =-5.6A		45	55	m Ω
Drain-Source On-State Resistance	Rds(on)	Vgs=-4.5V,ID=-4.2A		75	85	III 25
Forward Transconductance	gFS	V _{GS} =-5V,I _D =-5.6A		5		S
DAYNAMIC CHARACTERISTICS				,	•	
Input Capacitance	Ciss			582		pF
Output Capacitance	Coss	$V_{DS}=-15V, V_{GS}=0V$ f=1.0MHz		125		pF
Reverse Transfer Capacitance	Crss					pF
SWITCHING CHARACTERISISTICS					•	1
Turn-On Delay Time	td(on)	V _{DD} =-15V		9		ns
Rise Time	tr	ID=-5.6A,		10		ns
Turn-Off Delay Time	tD(OFF)	V _{GEN} =-4.5V R _L =10ohm		38		ns
Fall Time	tf	R _{GEN} =10ohm		23		ns
Total Gate Charge	Qg			11.7		nC
Gate-Source Charge	Qgs	V _{DS} =-15V,I _D =-1A V _{GS} =-10V		2.1		nC
Gate-Drain Charge	Qgd	v GS10 v		2.9		nC

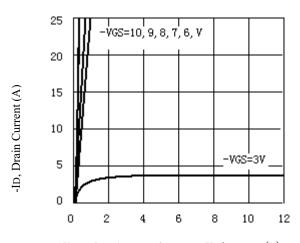
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ELECTRICAL CHARACTERICS (TA=25°C unless otherwise noted)

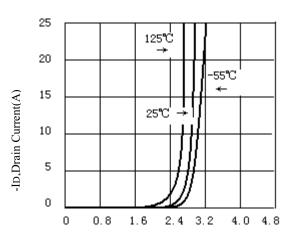
Parameter	Symbol	Condition	Min	Тур	Max	Unit			
DRAIN-SOURCE DIODE CHARACTERISTICS									
Diode Forward Voltage	Vsd	V _{GS} =0V,I _S =-1.7A		-0.84	-1.2	V			

Notes

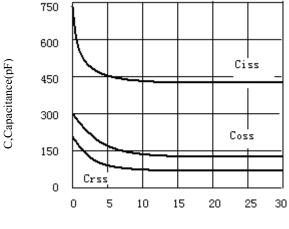
- a. Surface Mounted on FR4 Board, t≤10sec
- b. Pulse Test: Pulse Width ≤ 300Us, Duty Cycle ≤ 2%
- c. Guaranteed by design, not subject to production testing.



- VDS, Drain-to-Source Voltage (V) Figure 1.Output Characteristics



-VGS, Gate-to-source Voltage (V) Figure 2. Transfer Characteristics



- VGS, Drain-to Source Voltage Figure 3. Capacitance

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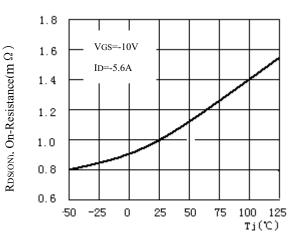
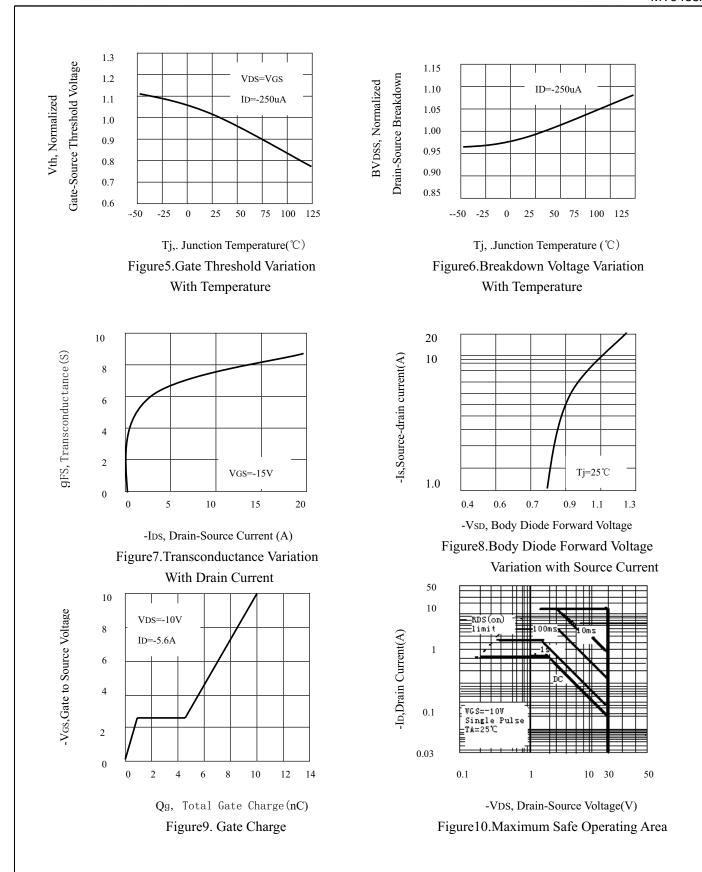


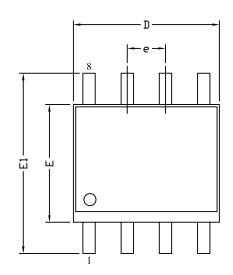
Figure 4. On-Resistance Variation with Temperature

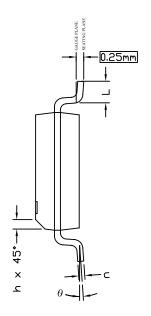


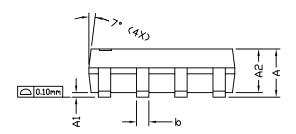
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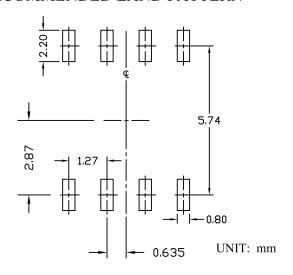
SO8 PACKAGE OUTLINE







RECOMMENDED LAND PATTERN

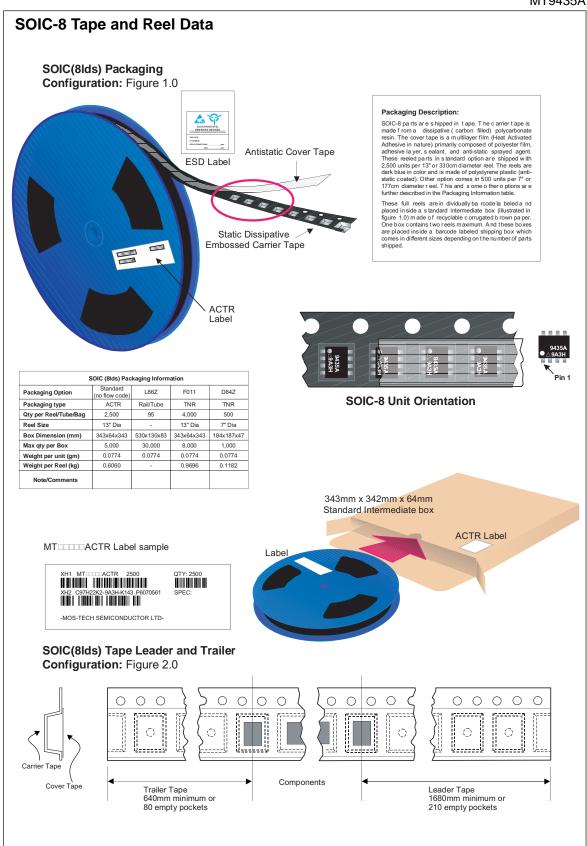


SYMBOLS	DIMENSIC	NS IN MILL	IMETERS	DIMENSIONS IN INCHES			
3 I MBOLS	MIN	NOM	MAX	MIN	NOM	MAX	
Α	1.35	1.65	1.75	0.053	0.065	0.069	
A1	0.10		0.25	0.004		0.010	
A2	1.25	1.50	1.65	0.049	0.059	0.065	
b	0.31		0.51	0.012		0.020	
c	0.17		0.25	0.007		0.010	
D	4.80	4.90	5.00	0.189	0.193	0.197	
Е	3.80	3.90	4.00	0.150	0.154	0.157	
e	1	.27 BSC		0.050 BSC			
E1	5.80	6.00	6.20	0.228	0.236	0.244	
h	0.25		0.50	0.010		0.020	
L	0.40		1.27	0.016		0.050	
θ	00		80	00		80	

NOTE

- 1. ALL DIMENSIONS ARE IN MILLMETERS.
- 2. DIMENSIONS ARE INCLUSIVE OF PLATING.
- 3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- 4. DIMENSION L IS MEASURED IN GAUGE PLANE.
- 5. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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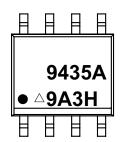


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Part Marking Information

SO-8 (PMG Code)

SO-8 Devices



9435A = Example Base Part Number

• = Pin 1 Indicator

△ = ESD Symbol 🖾

9 = Year Code

A = Month Code

3 = Week Code

H = Assembly Factory Code

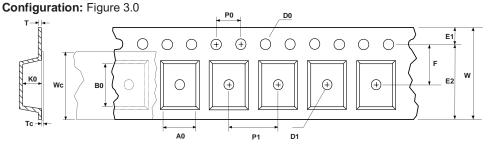
NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

SOIC-8 Tape and Reel Data, continued

SOIC(8lds) Embossed Carrier Tape



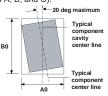
User Direction of Feed	
	$\overline{}$

Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



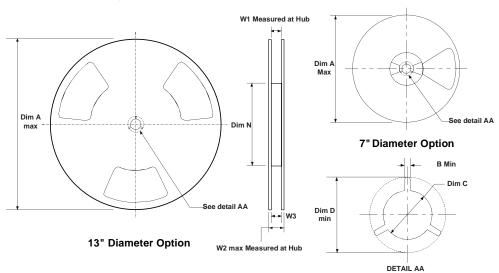
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



	Dimensions are in inches and millimeters										
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)		
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4		
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4		

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